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PCB

Compal Confidential

NDWG0 Schematics Document

AMD S1g3/ RS880M/ SB710

2009 / 09 / 22

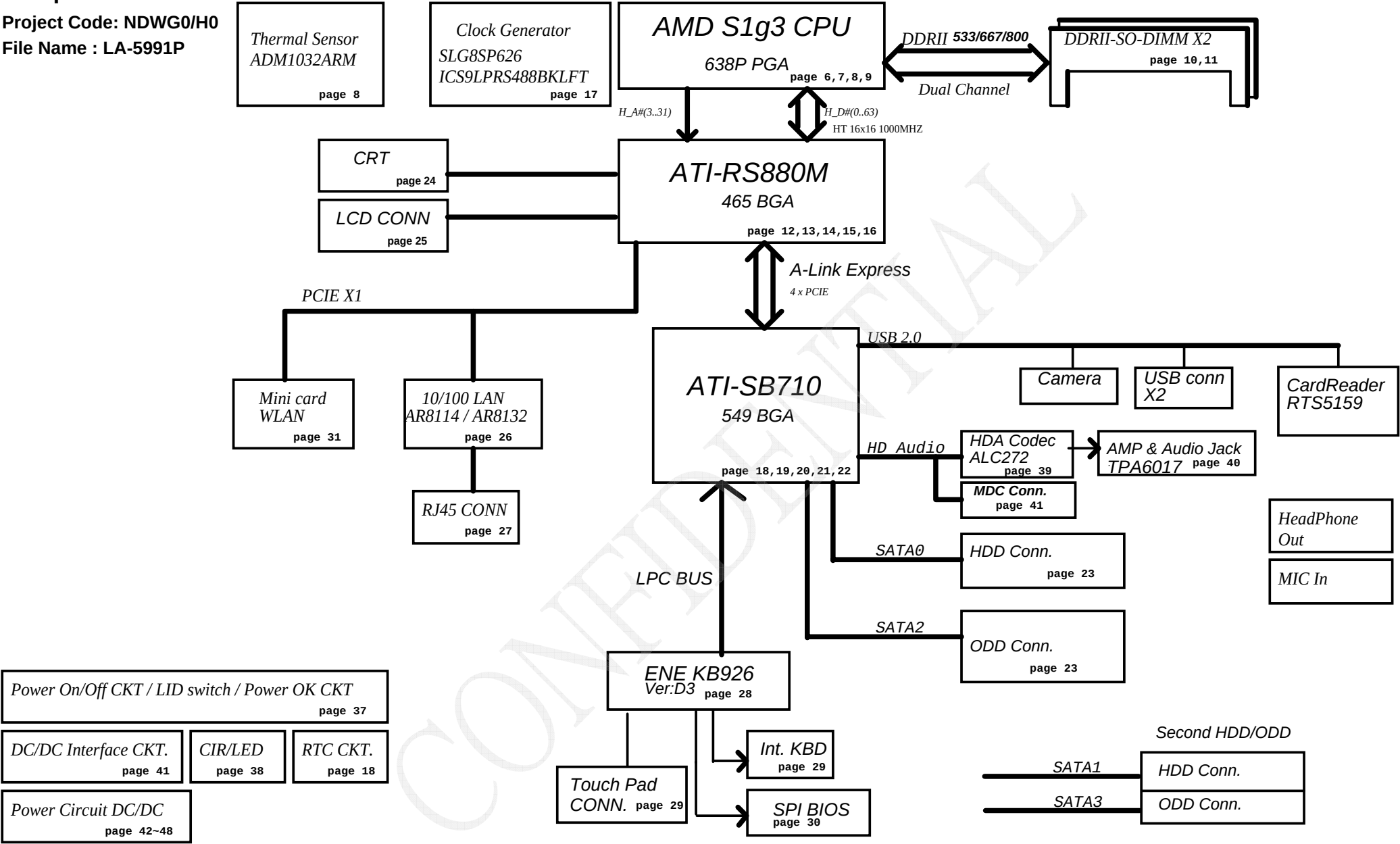
LA-5991P

Rev: 0.1

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Project Code: NDWG0/H0
File Name : LA-5991P



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VIN	Adapter power supply (19V)			
B+	AC or battery power rail for power circuit.			
+CPU_CORE	Core voltage for CPU			
+0.9V	0.9V switched power rail for DDR terminator			
+1.2V_HT	1.2V switched power rail	ON	OFF	
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON		ON*
+1.8VS	1.8V switched power rail		OFF	
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

Device	Address	Device	Address
Clock Generator	1101 001Xb	New Card	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Wireless Lan			

Device	Address
ADM1032	1001 100X b

Device	Address
New Card	

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

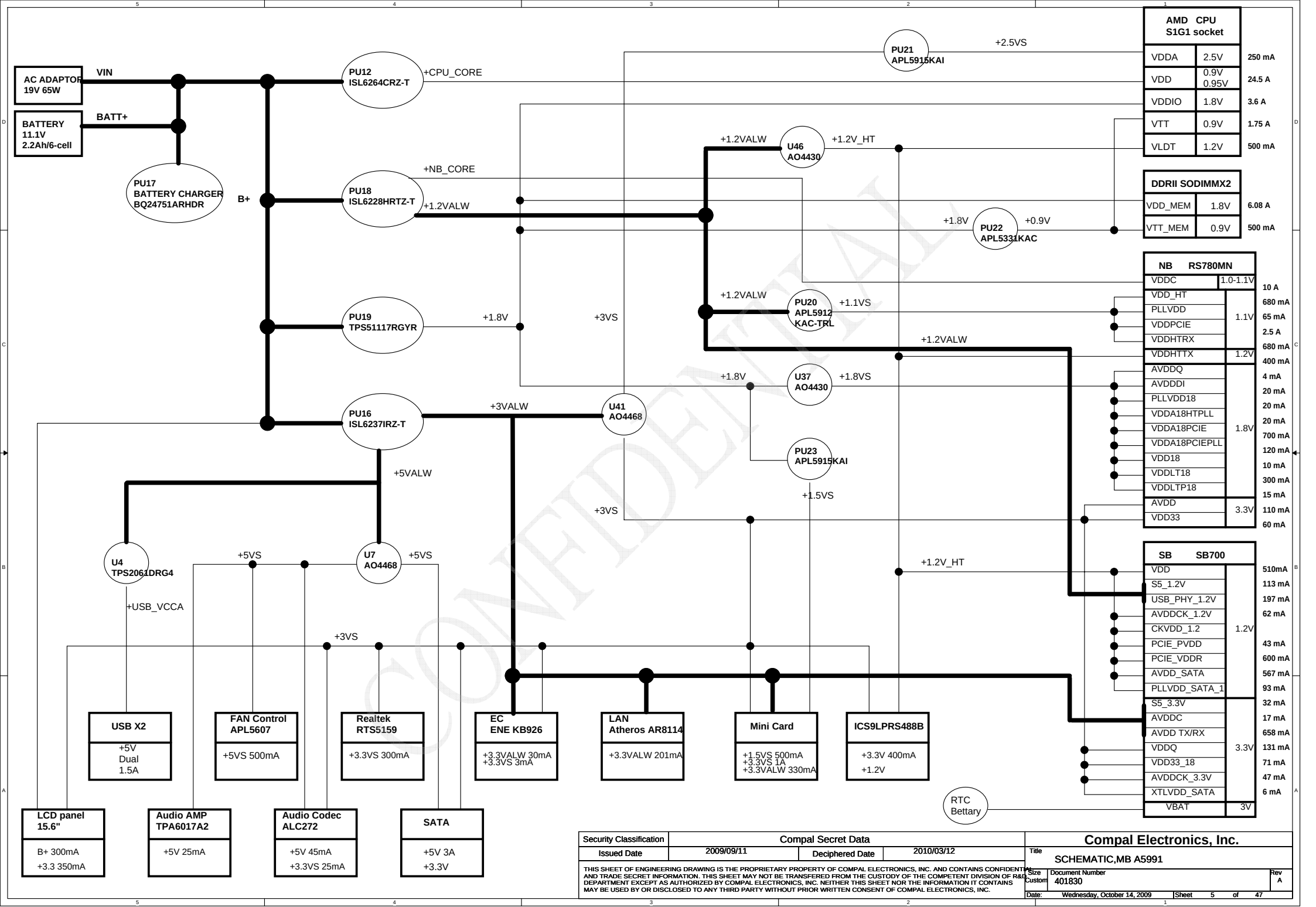
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	No Support VaryBright
1	
2	
3	Support VaryBright
4	
5	
6	
7	

SKU ID	SKU
0	NCWG0
1	
2	
3	NAL00
4	
5	
6	
7	NCWH0

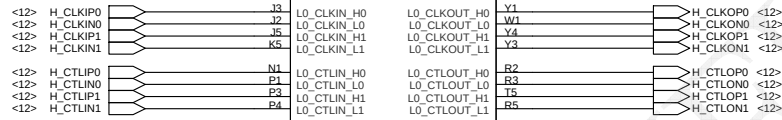
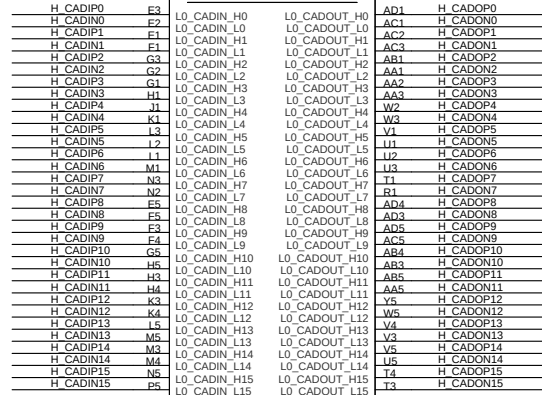
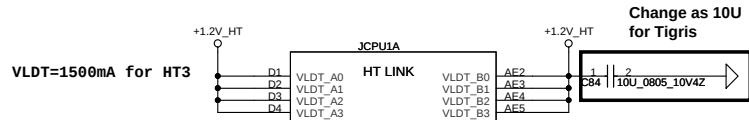
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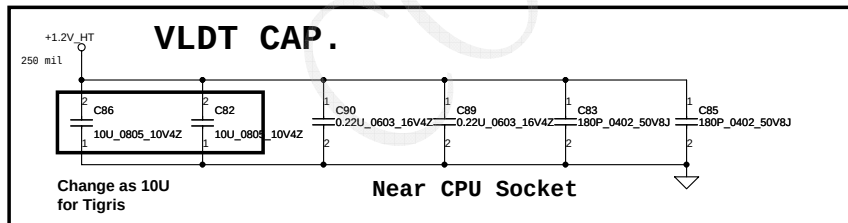
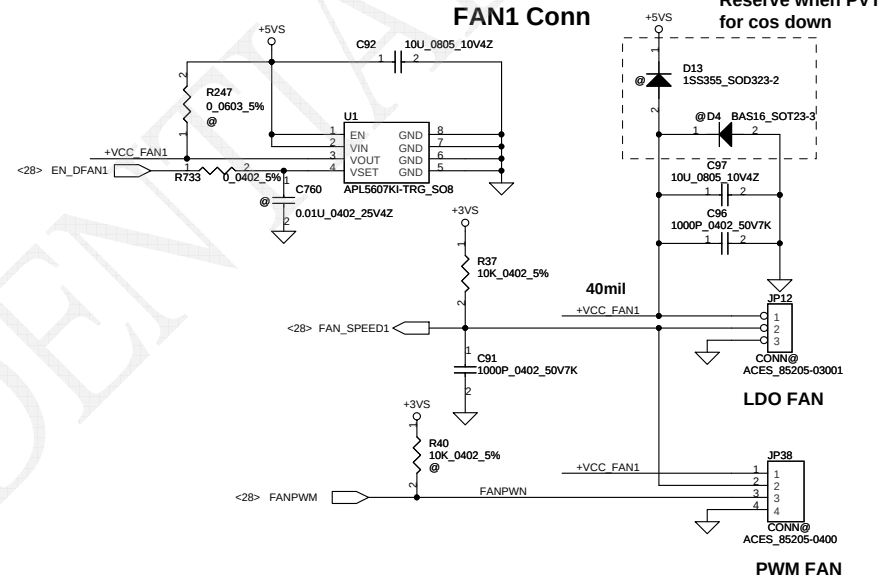


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 <12> H_CADIN[0..15] H_CADIN[0..15]

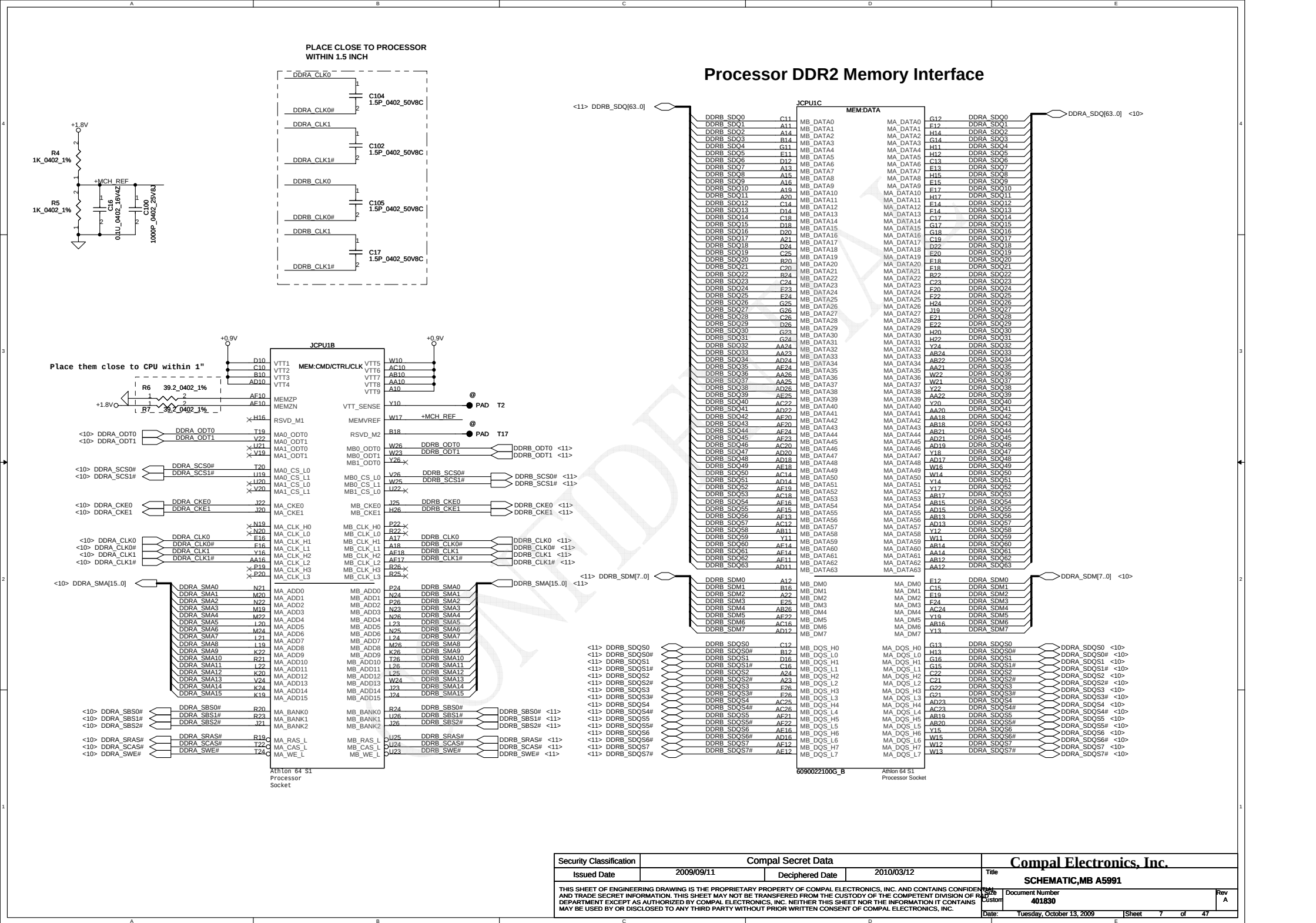
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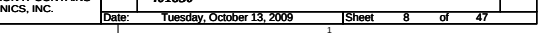
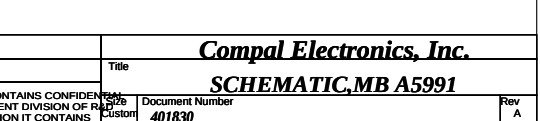
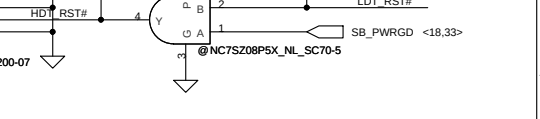
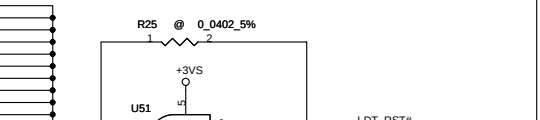
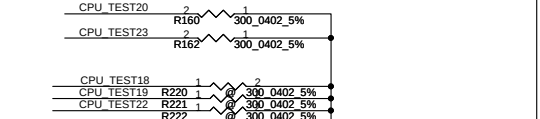
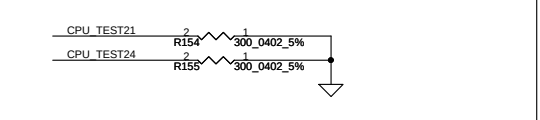
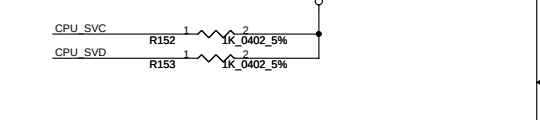
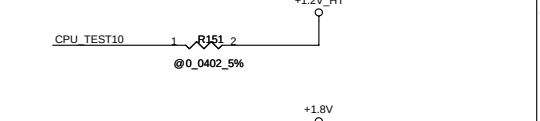
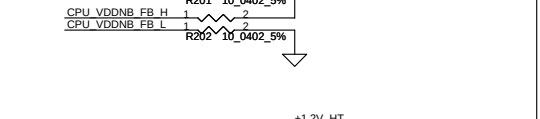
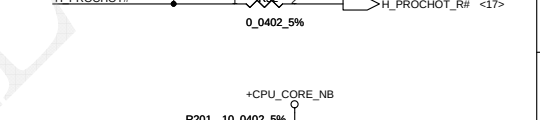
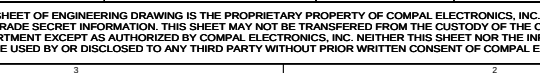
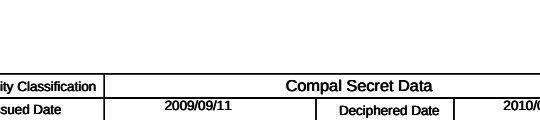
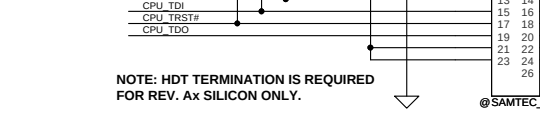
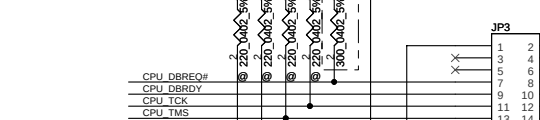
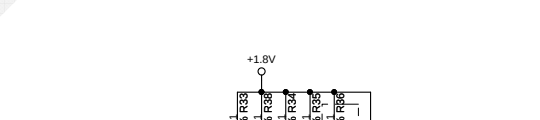
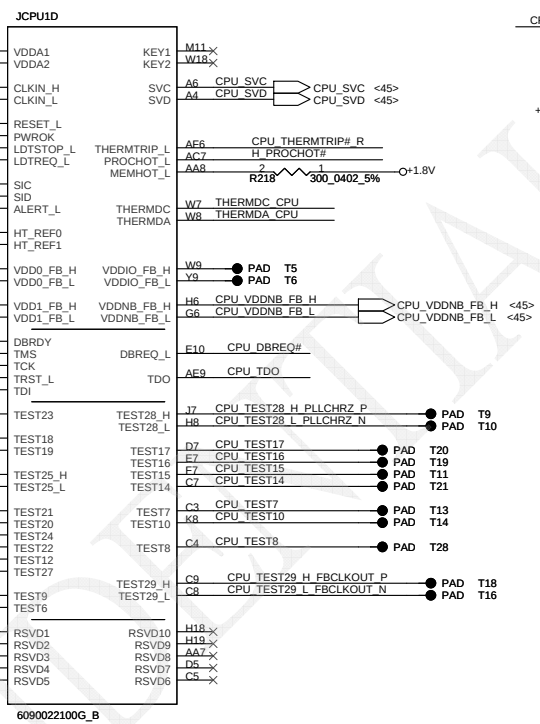
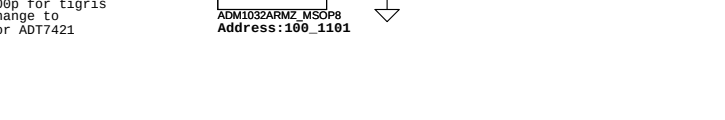
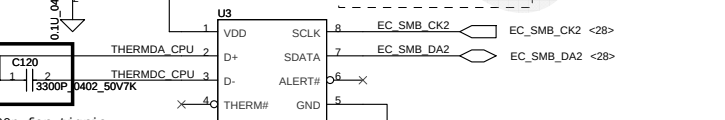
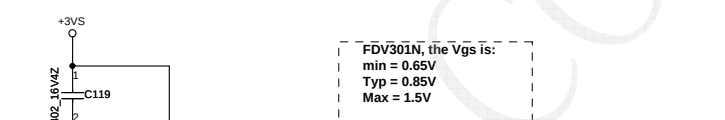
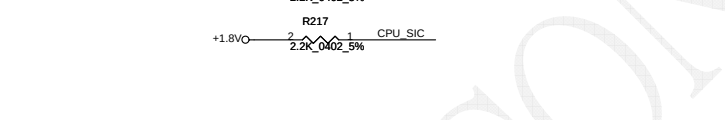
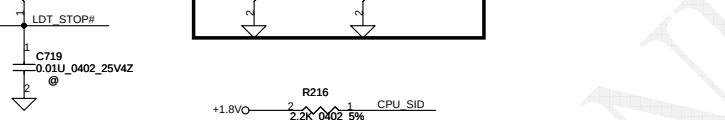
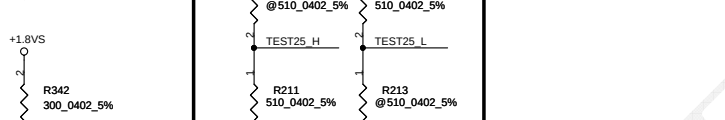
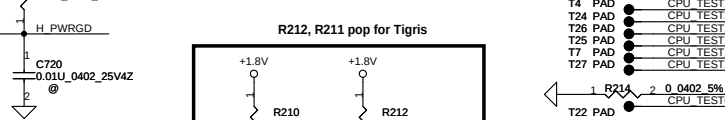
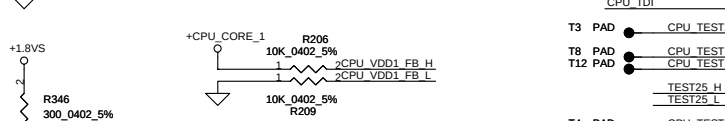
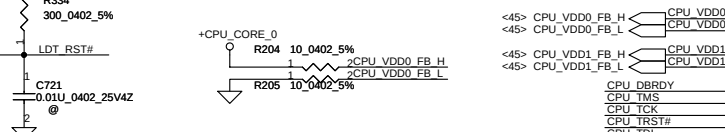
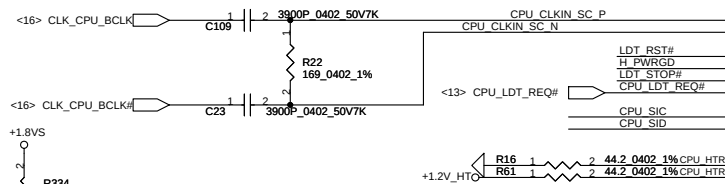
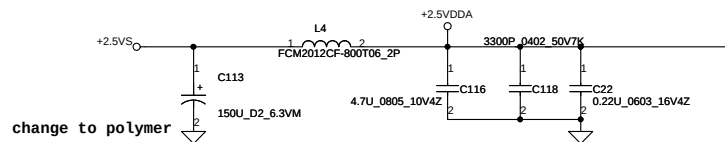
6090022100G_B
 Athlon 64 S1
 Processor Socket



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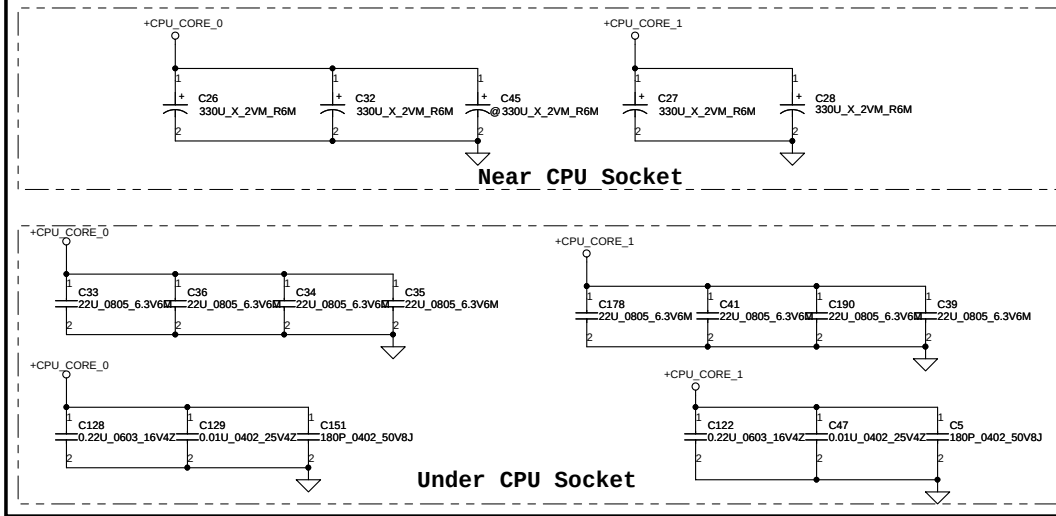


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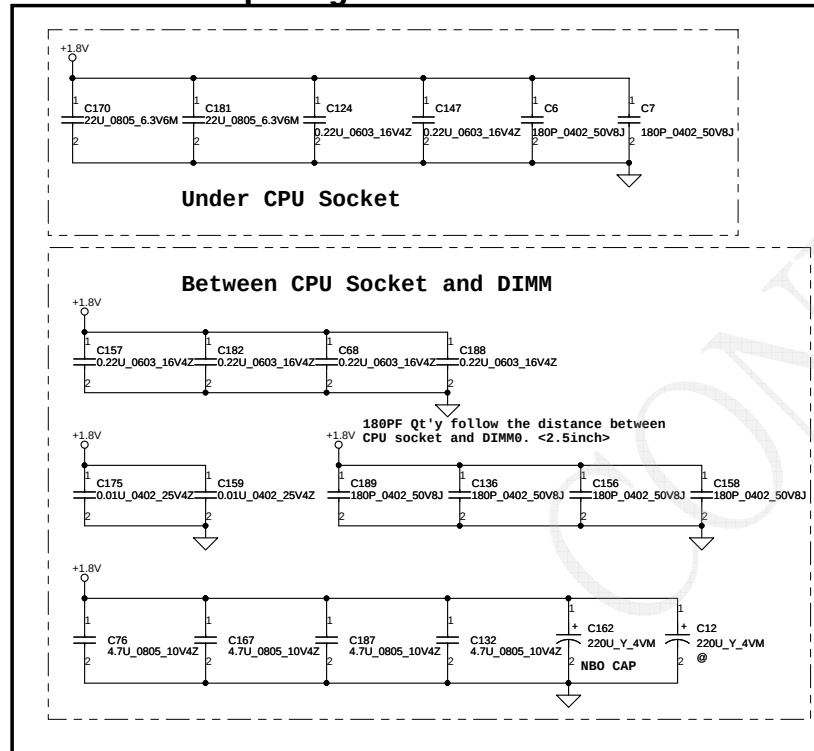


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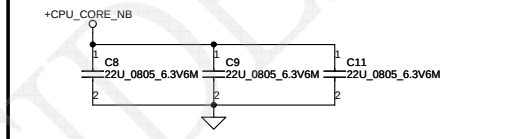
VDD(+CPU_CORE) decoupling.



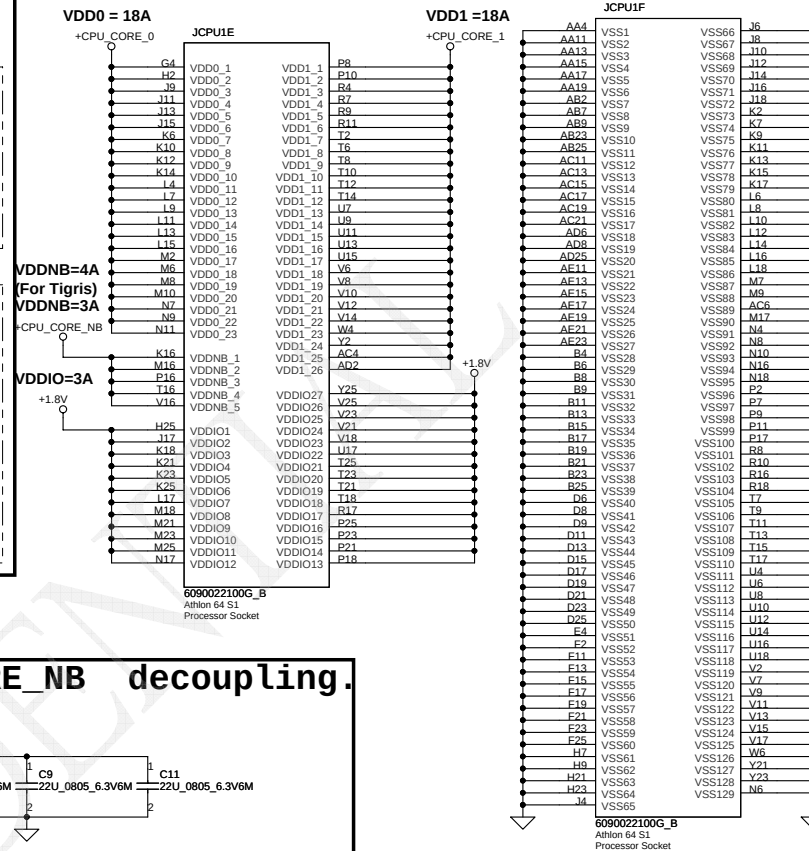
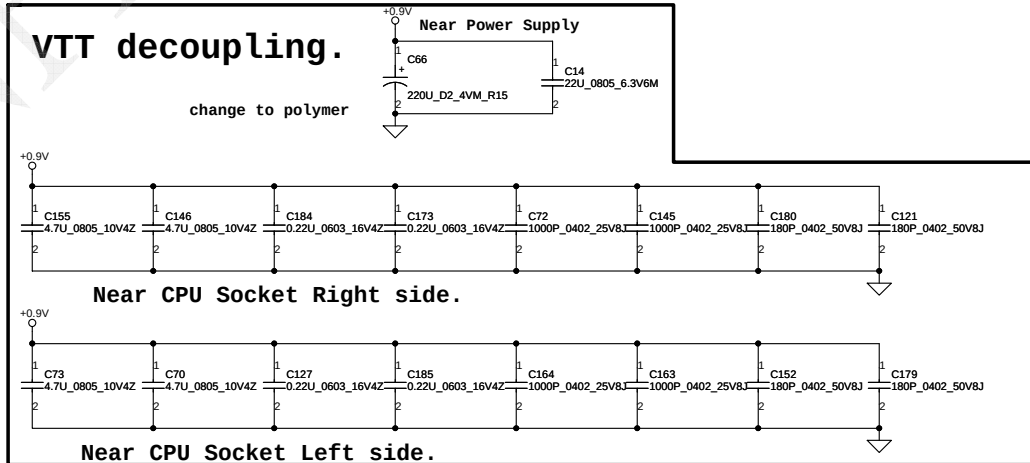
VDDIO decoupling.



+CPU_CORE_NB decoupling.



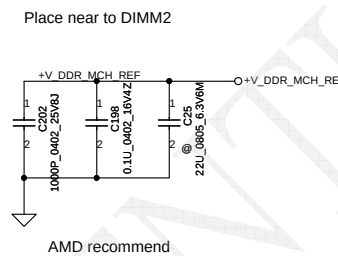
VTT decoupling.



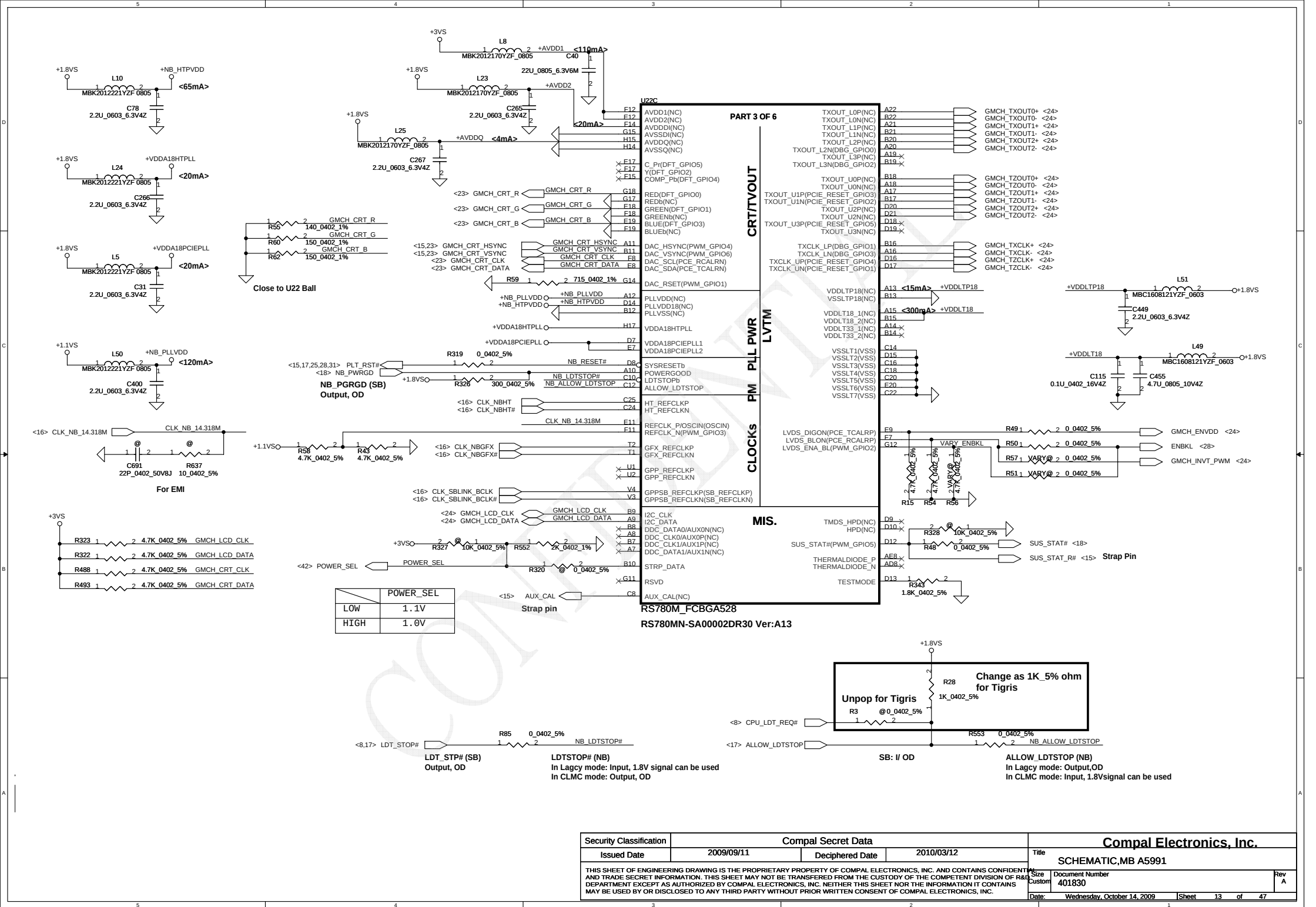
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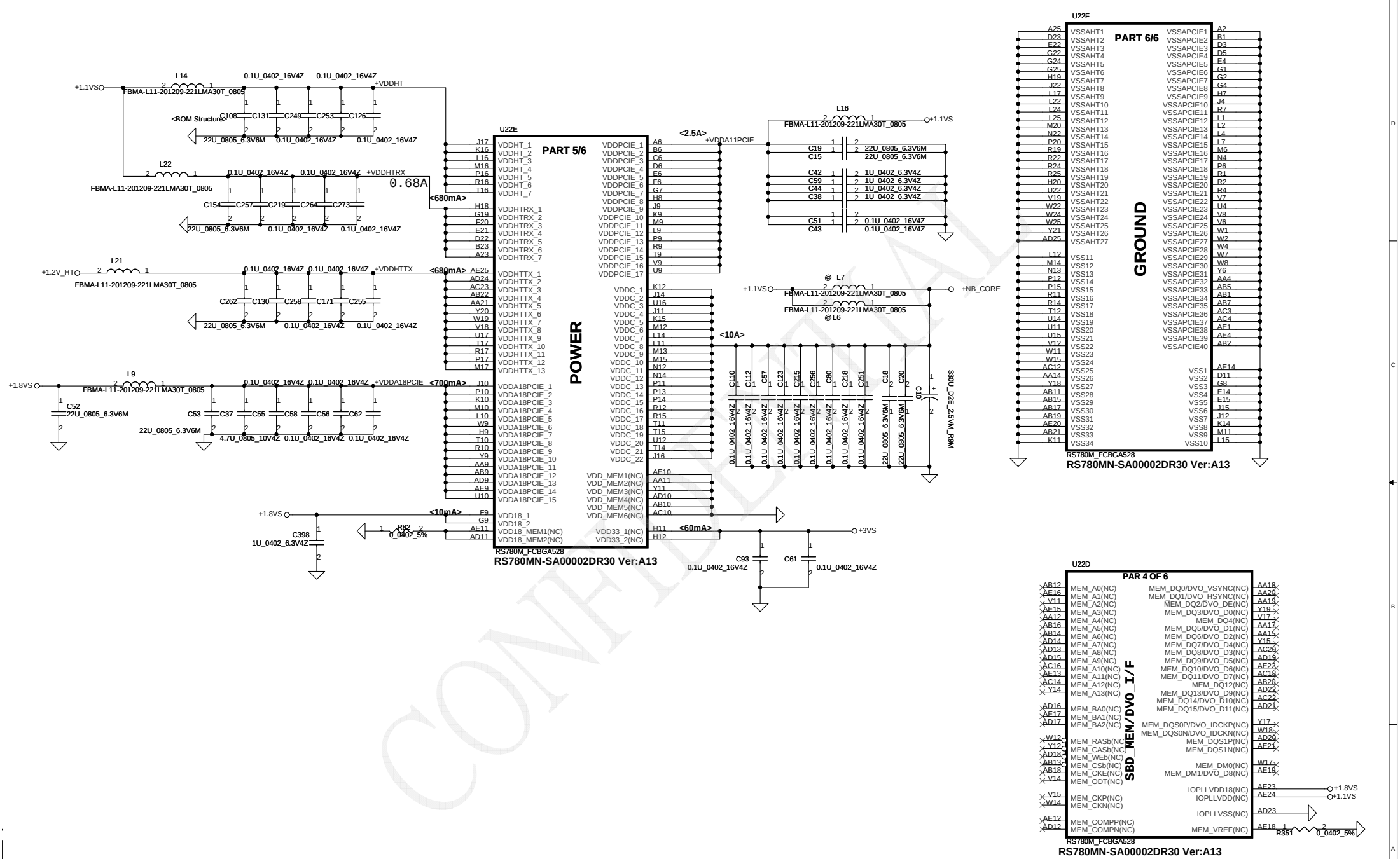
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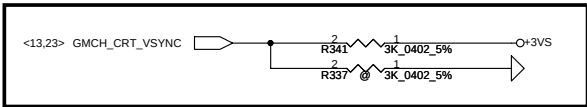


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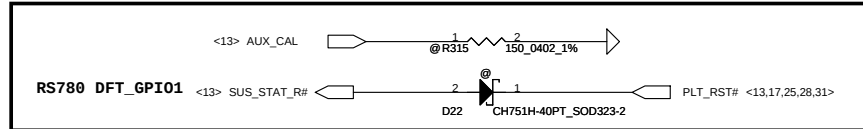


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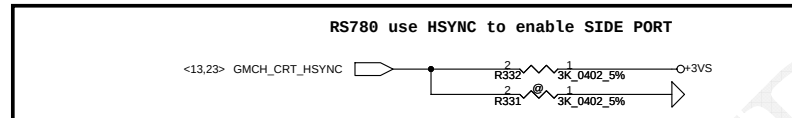
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

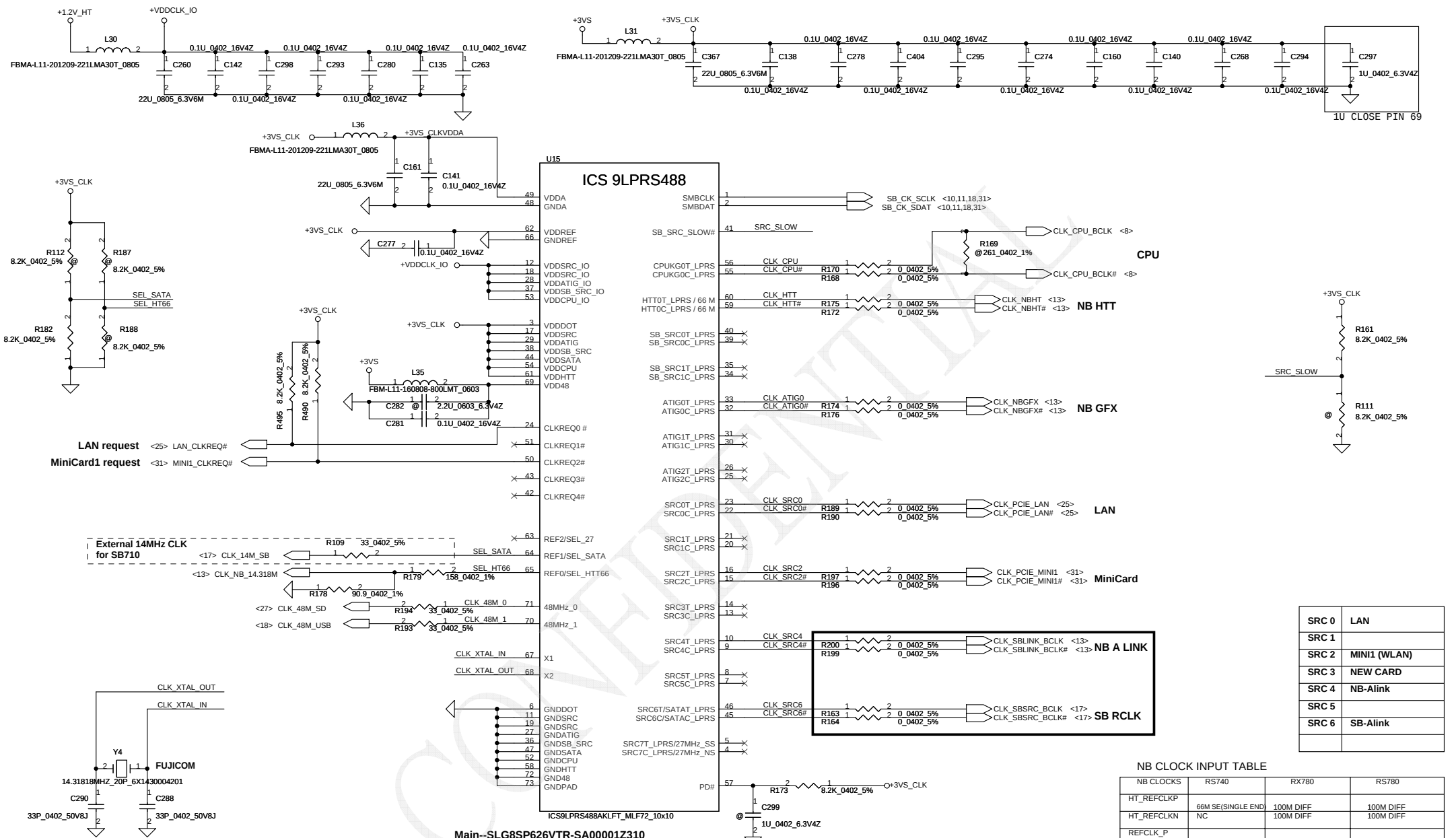
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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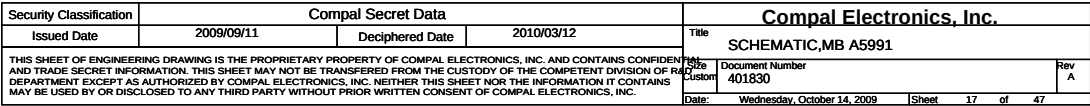


SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

* default

SEL_27M No used	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

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Main
HDD

2nd
HDD

Main
ODD

2nd
ODD

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<22> SATA_DTX_C_SRX_P1
<22> SATA_STX_DRX_P2
<22> SATA_STX_DRX_N2
<22> SATA_DTX_C_SRX_N2
<22> SATA_DTX_C_SRX_P2
<22> SATA_STX_DRX_P3
<22> SATA_STX_DRX_N3
<22> SATA_DTX_C_SRX_N3
<22> SATA_DTX_C_SRX_P3

U10B

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

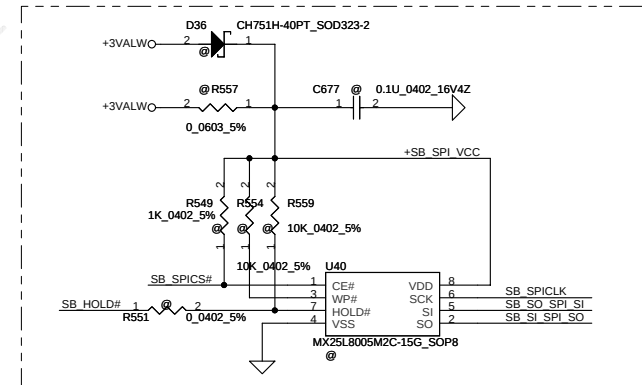
SPI ROM

HW MONITOR

SATA PWR

218S7EALA11FG_BGA528_SB700
SA00001S570 Ver:A12

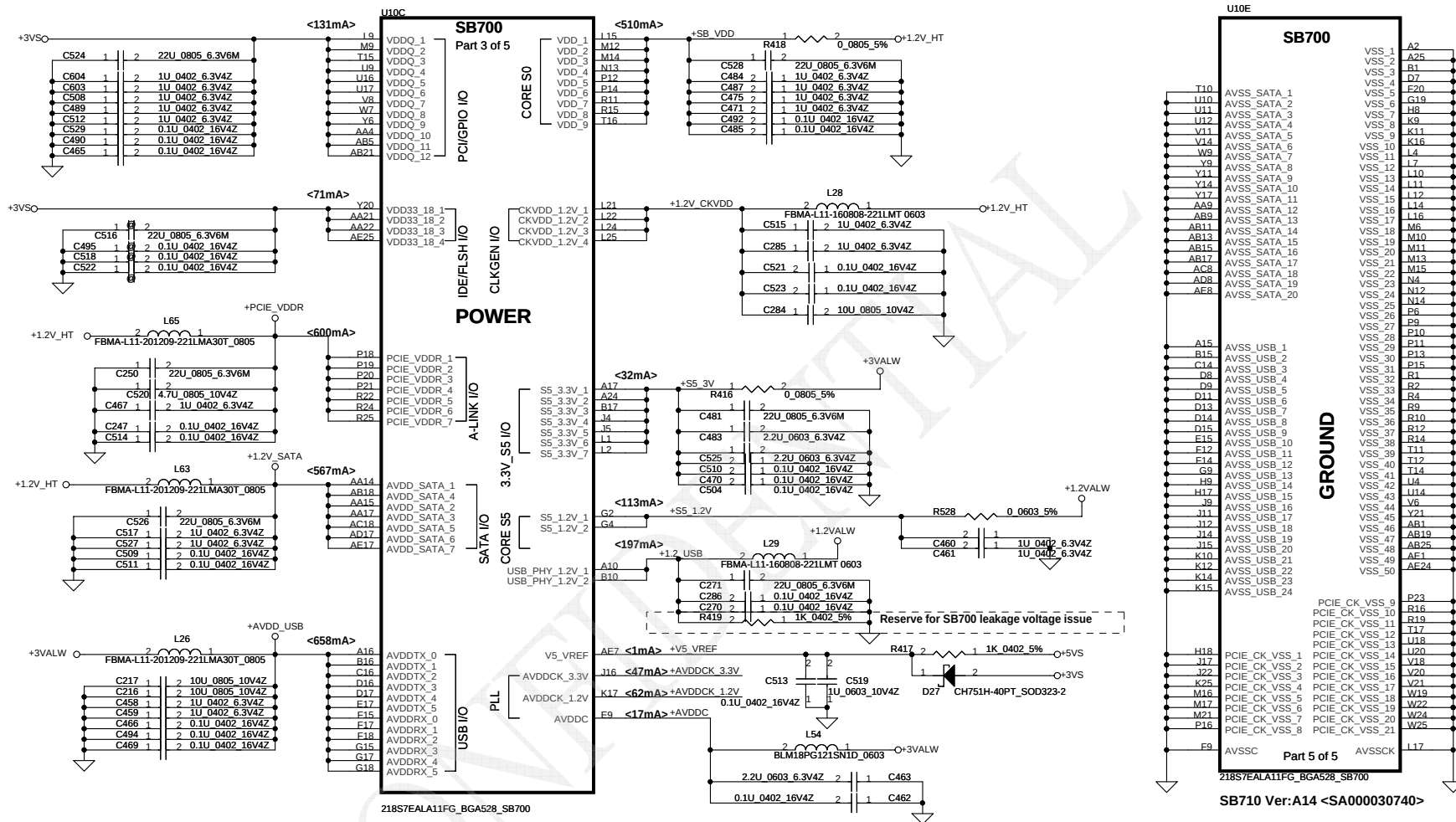
Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller



Reserve For Debug

for ACIN level issue

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								Size		Document Number	
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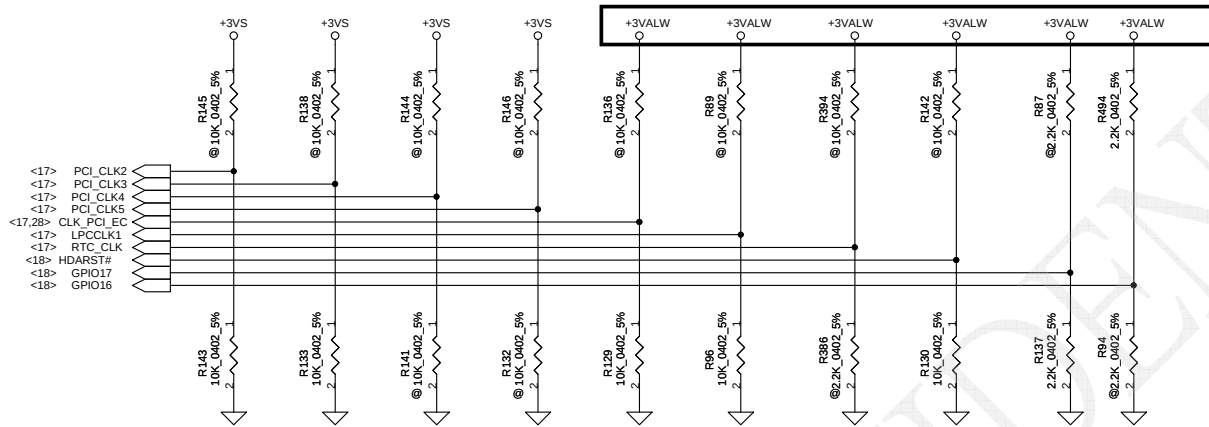


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM

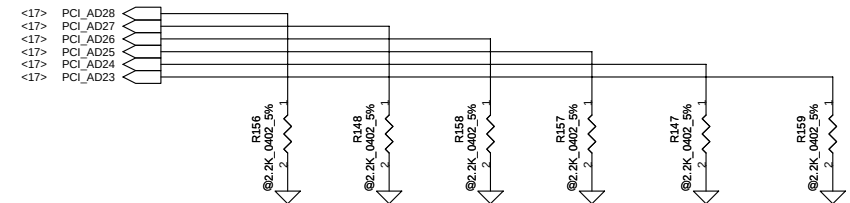


DEBUG STRAPS

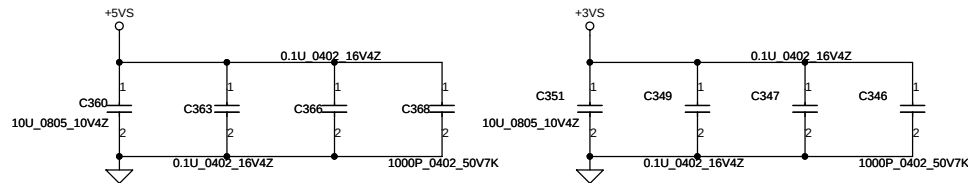
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

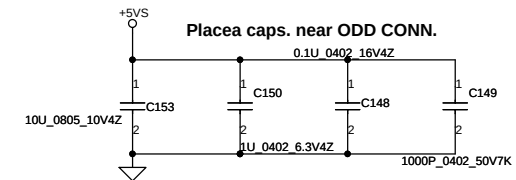
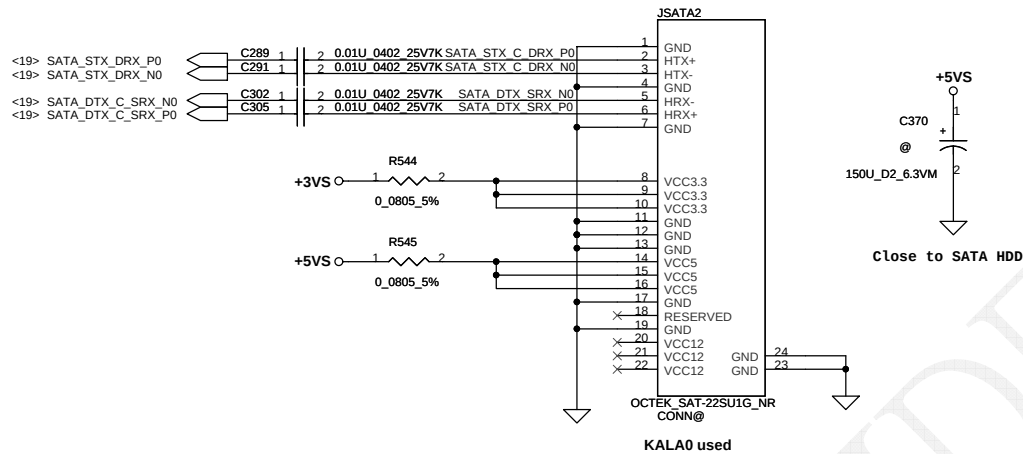
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



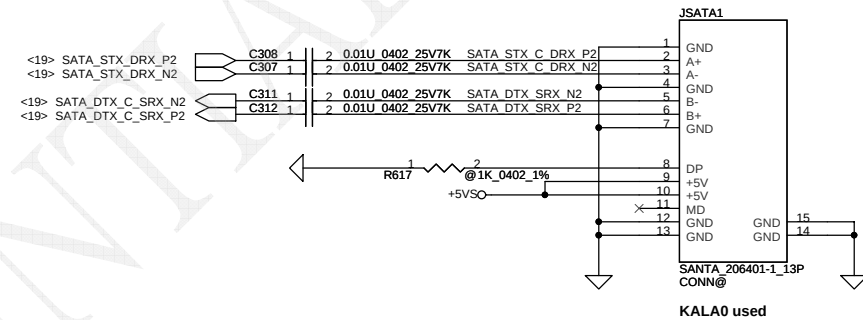
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SATA HDD CONN

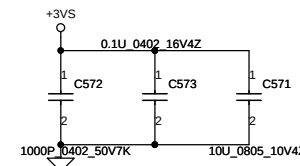
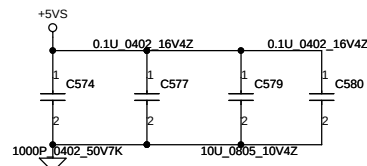
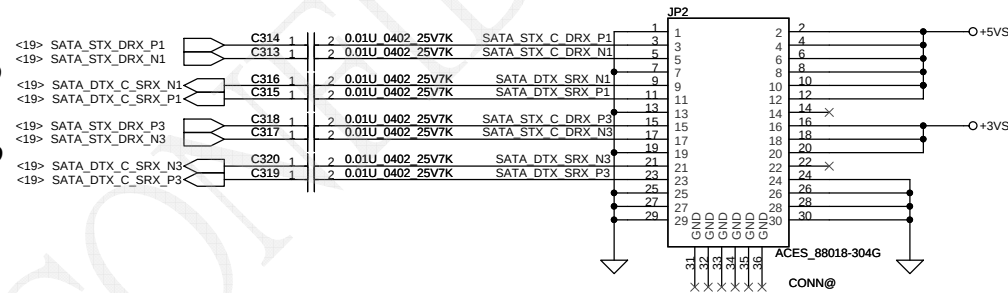


SATA ODD CONN



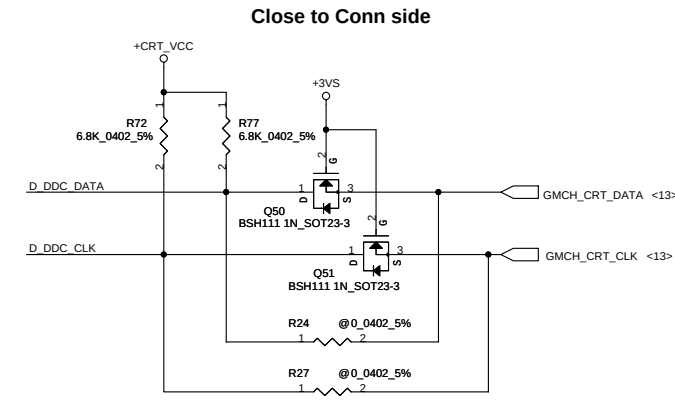
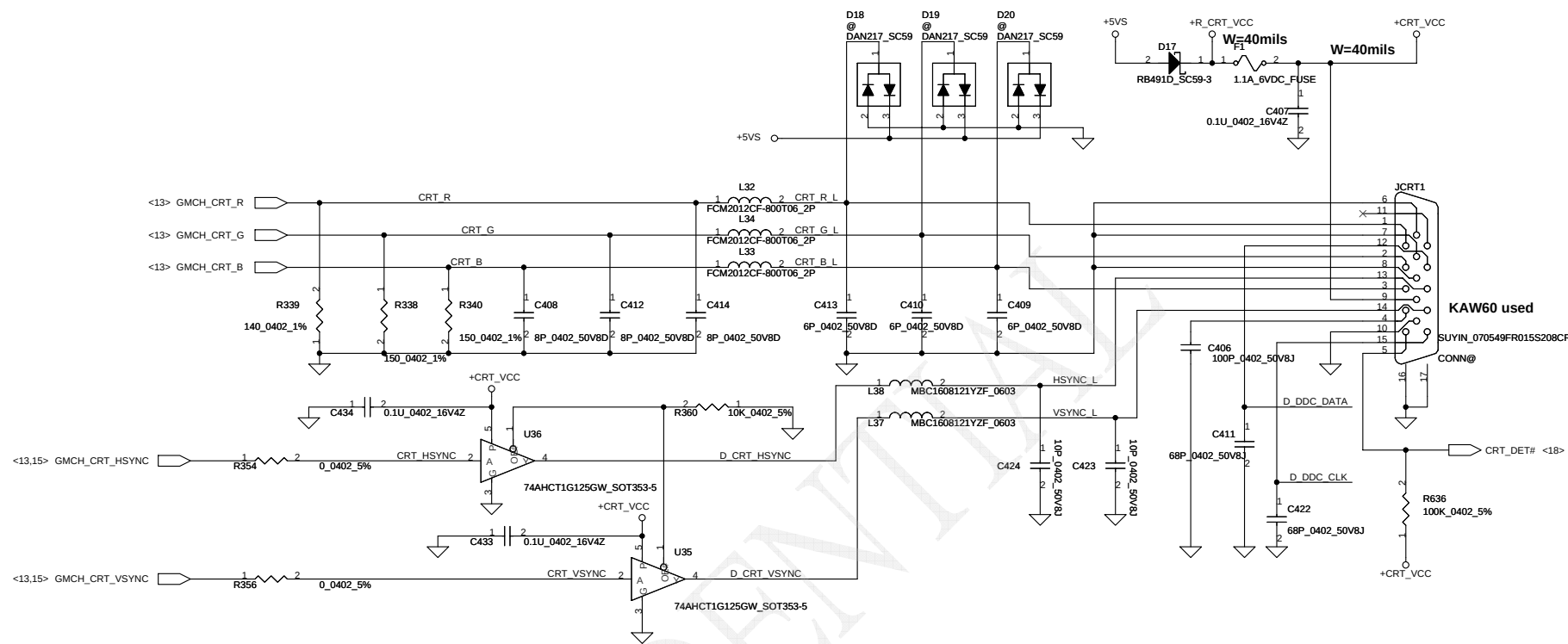
Second HDD

Second ODD



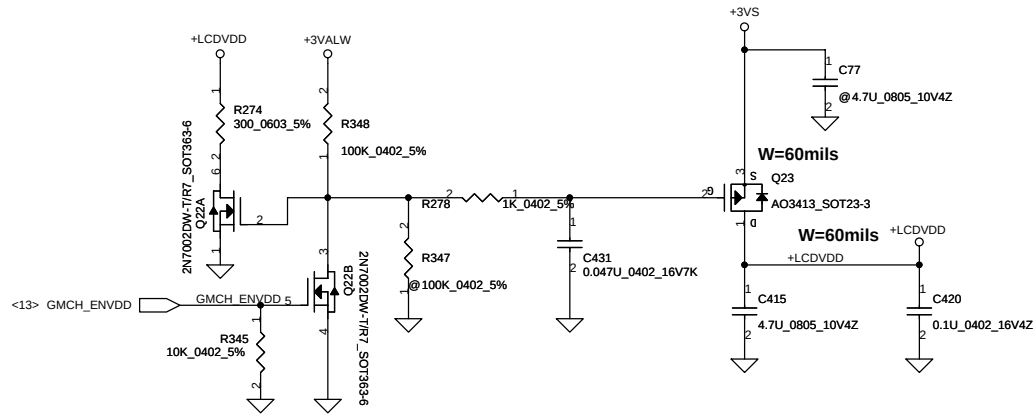
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CRT Connector

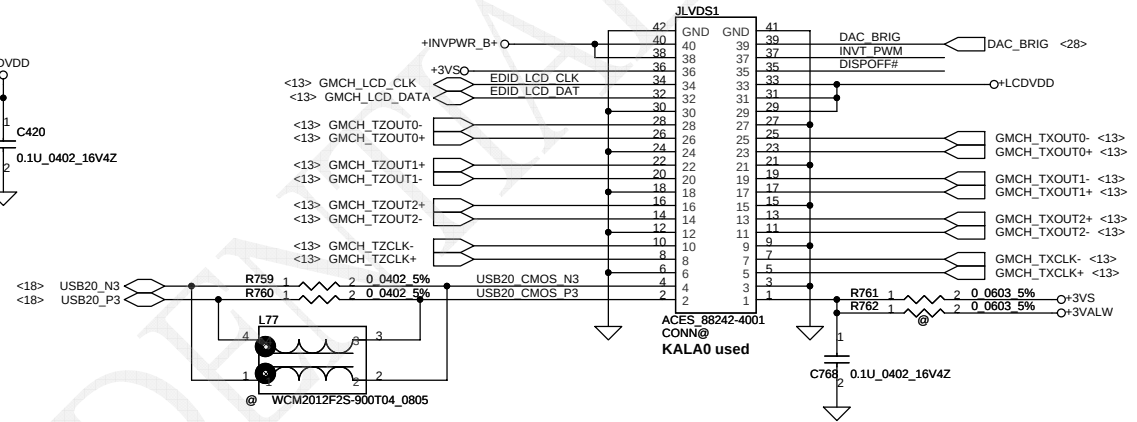


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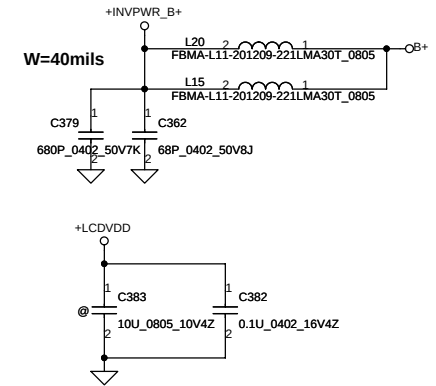
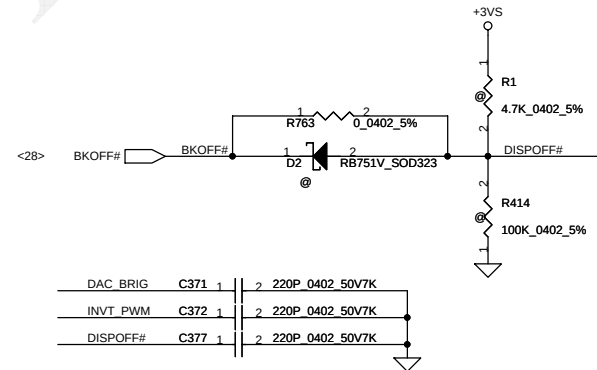
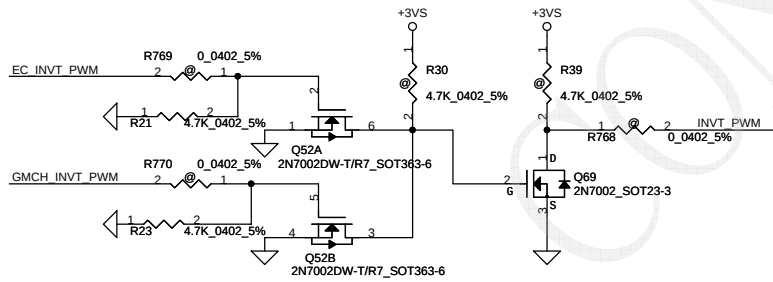
LCD POWER CIRCUIT



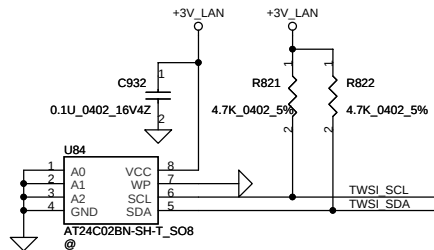
LCD/PANEL CONN.



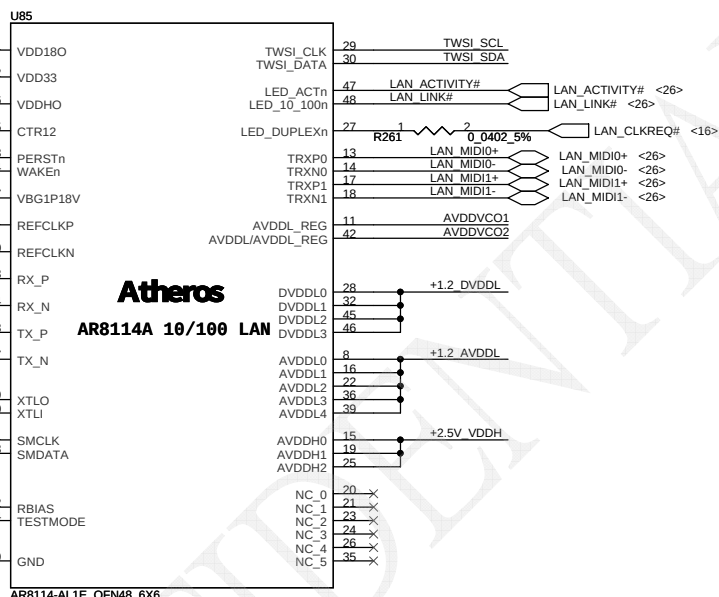
VARYBRIGHT FUNCTION



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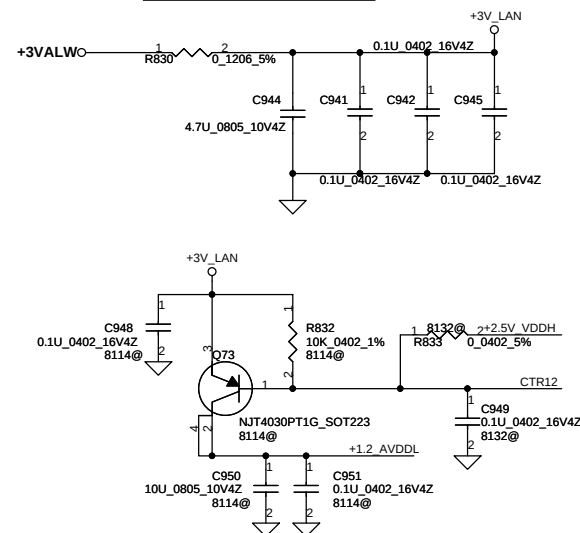
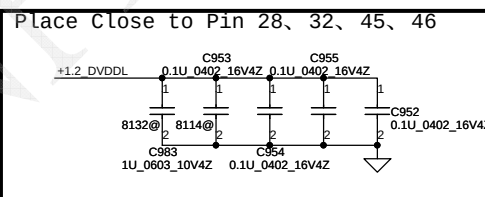


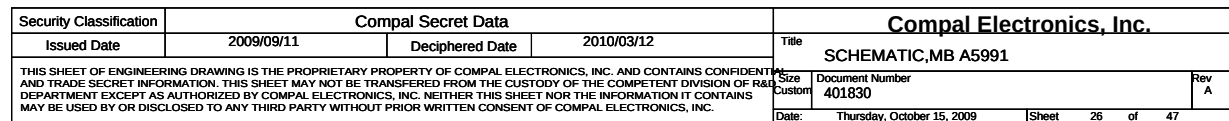
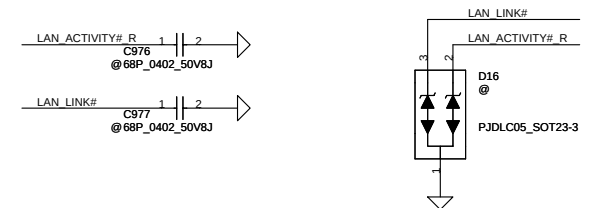
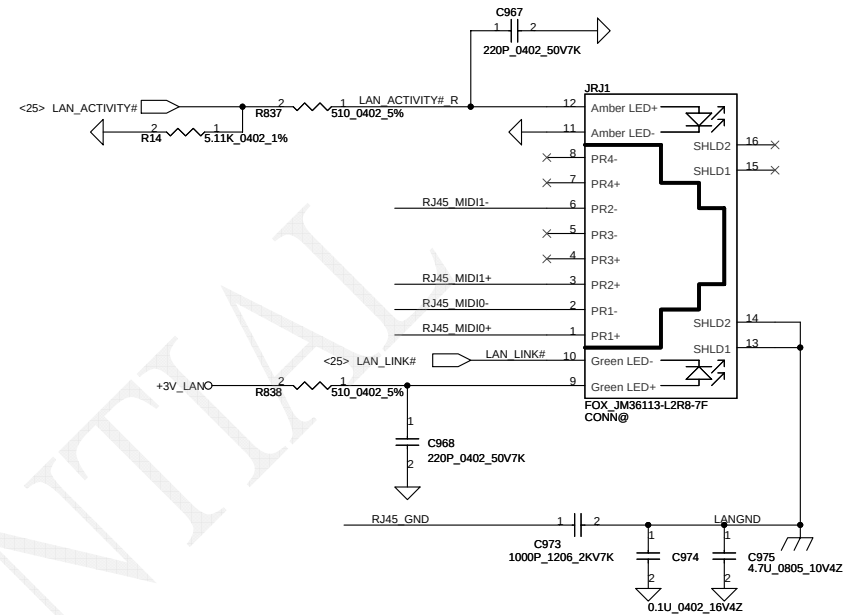
LAN	MDIO+	R643	2	1	49.9	0402	1%	C978	1	2	0.1U	0402	16V4Z
LAN	MDIO-	R645	2	1	49.9	0402	1%						
LAN	MDIO+	R846	2	1	49.9	0402	1%	C979	1	2	0.1U	0402	16V4Z
LAN	MDIO-	R847	2	1	49.9	0402	1%						

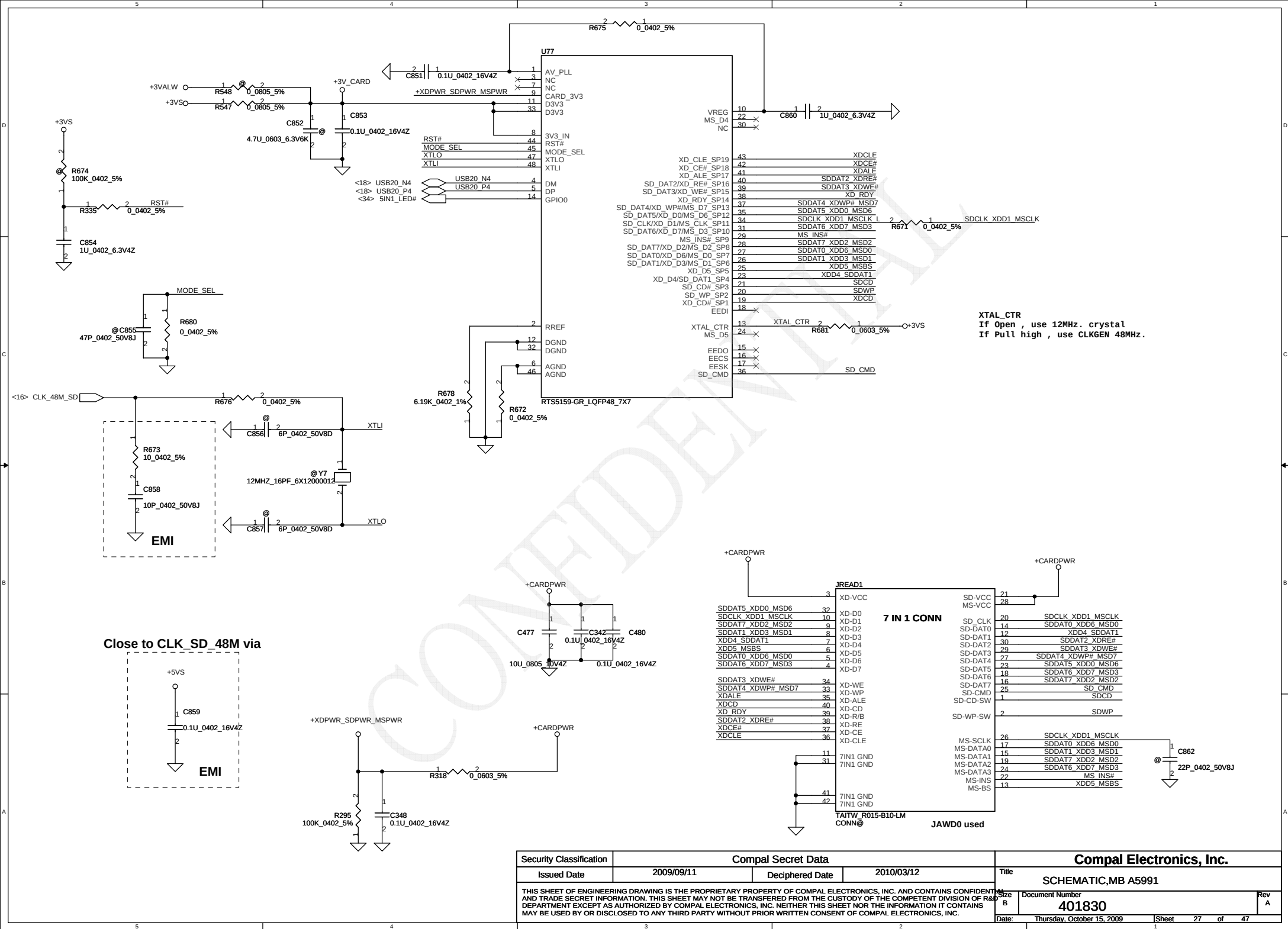


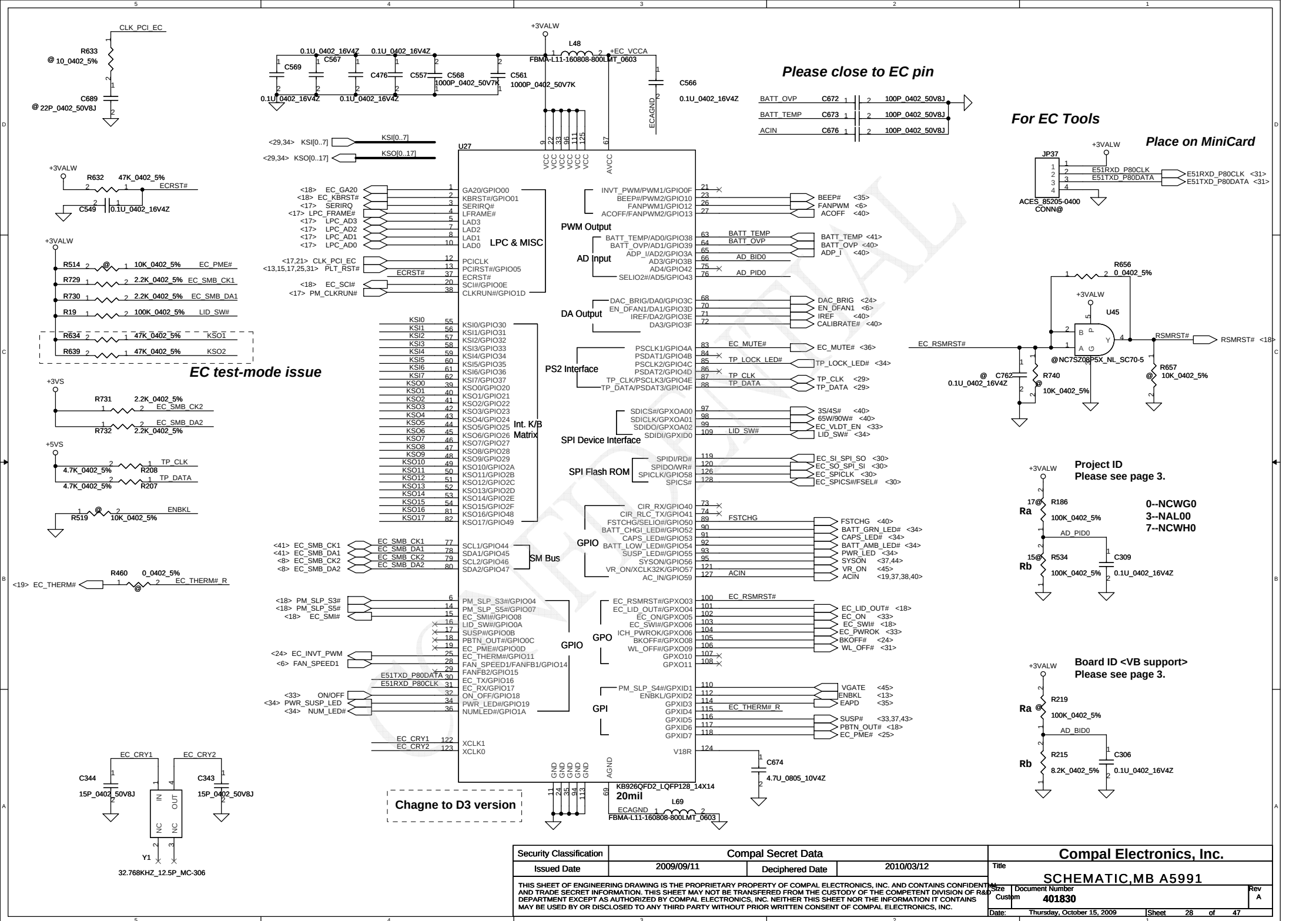
C943	0.10 040
------	----------

Place Close to Chip

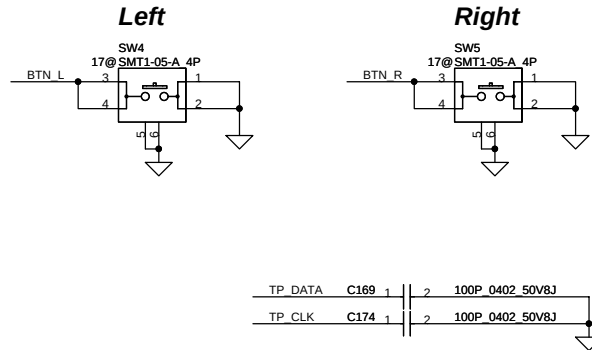




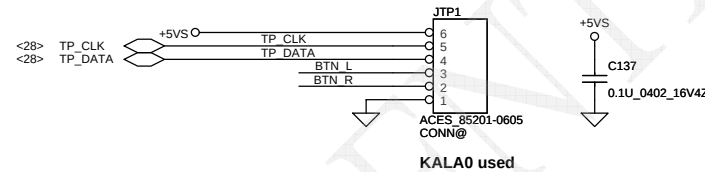




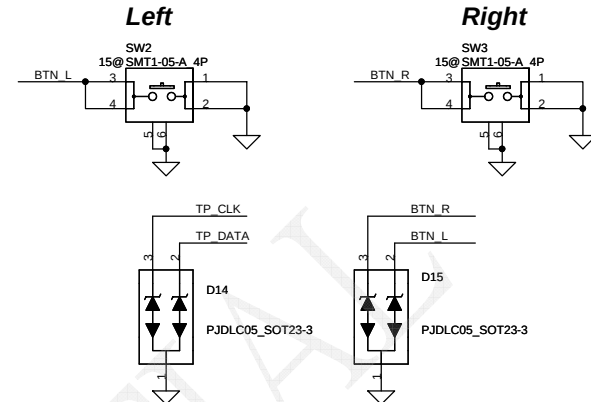
For 17"



To TP/B Conn.

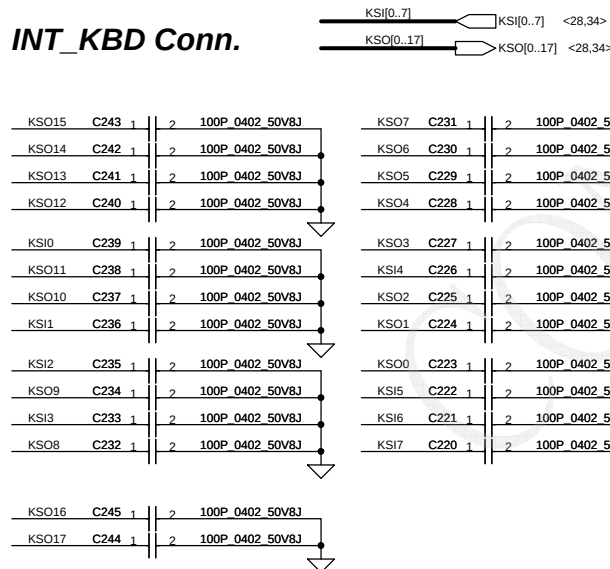


For 15"

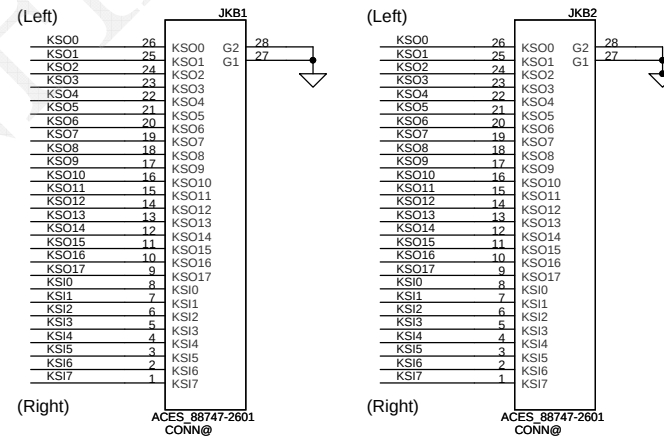


Change to SCA00000200

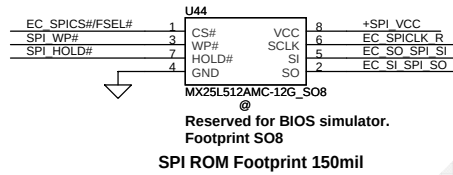
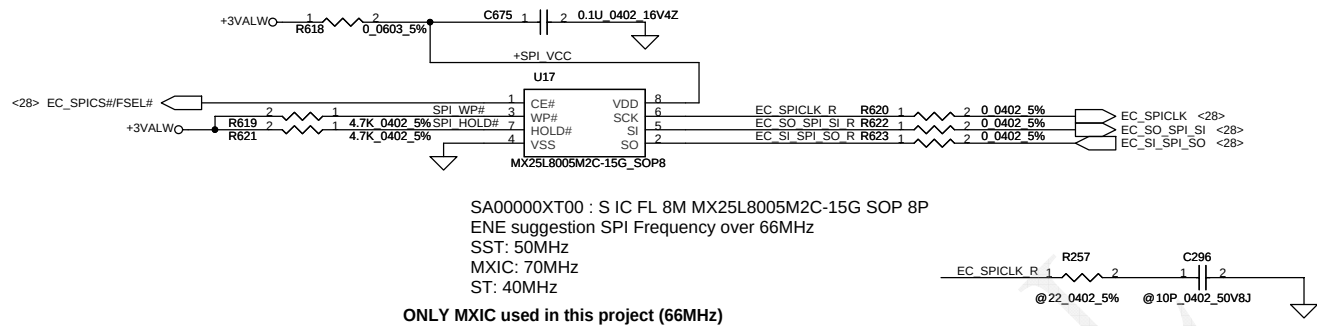
INT_KBD Conn.



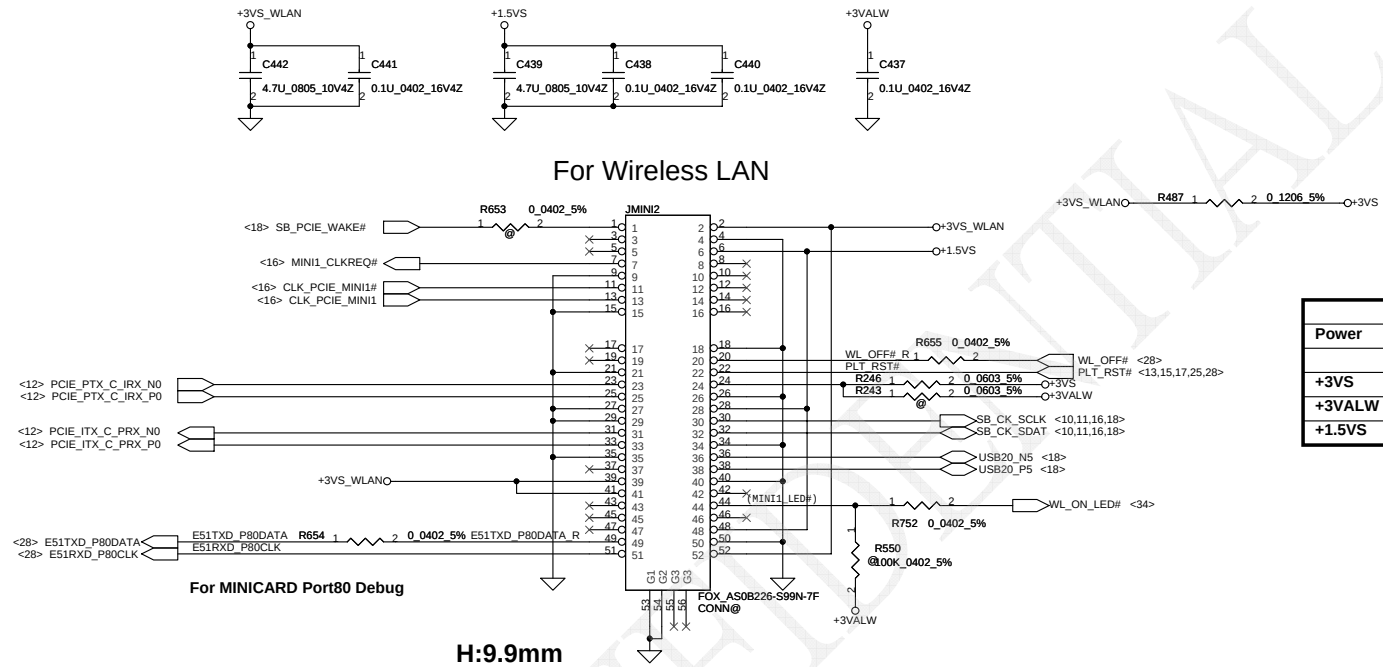
KB1 for 15"
KB2 for 17"



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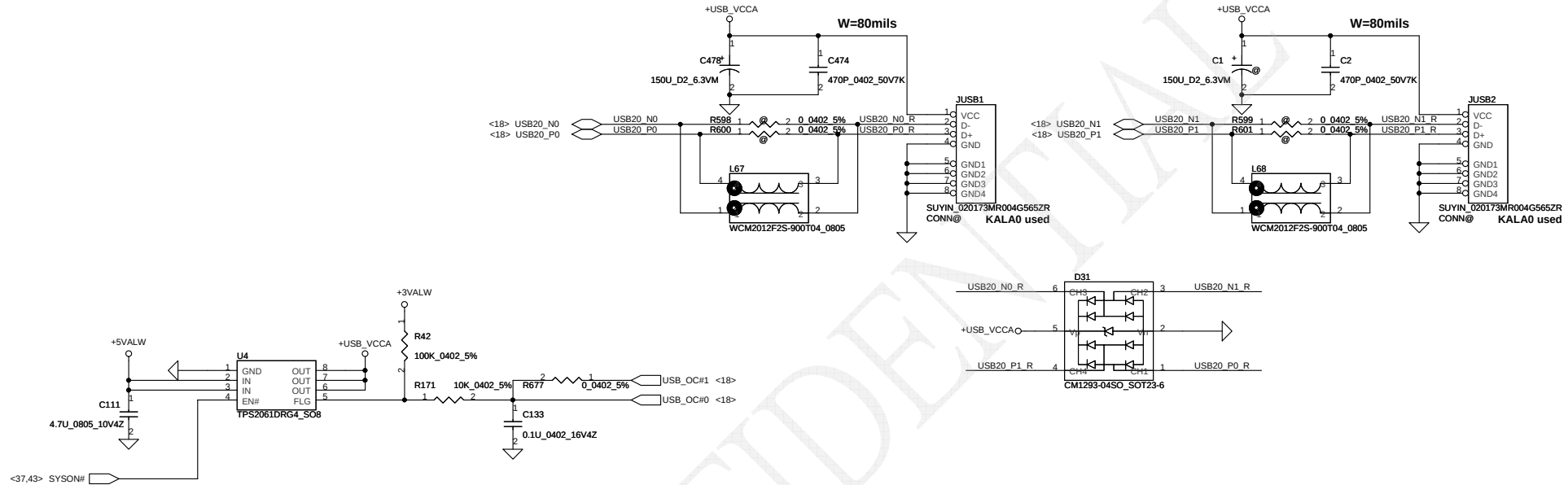


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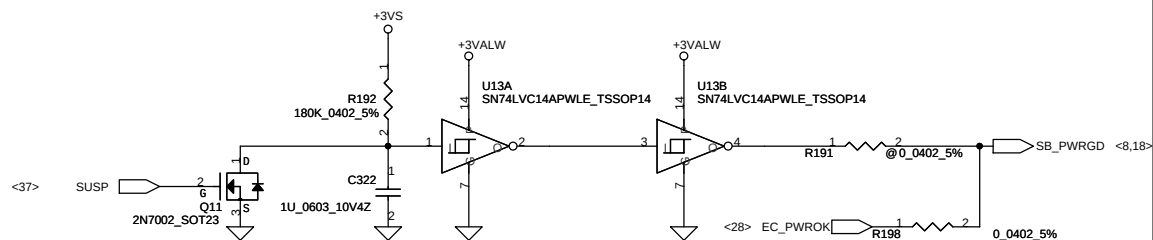
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

USB CONN. 1 & 2

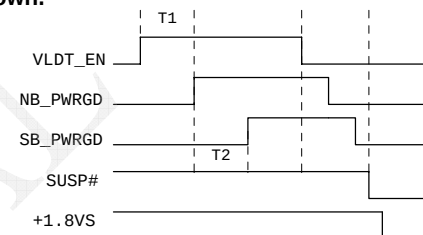


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										Document Number		Rev A	
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										Date		Thursday, October 15, 2009	
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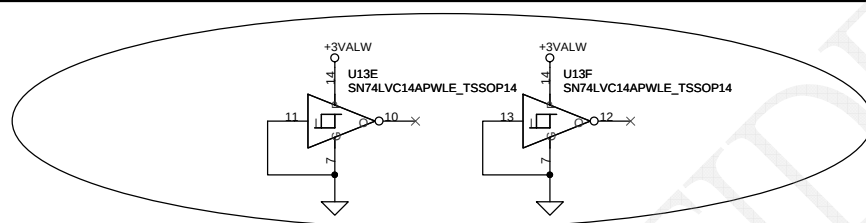
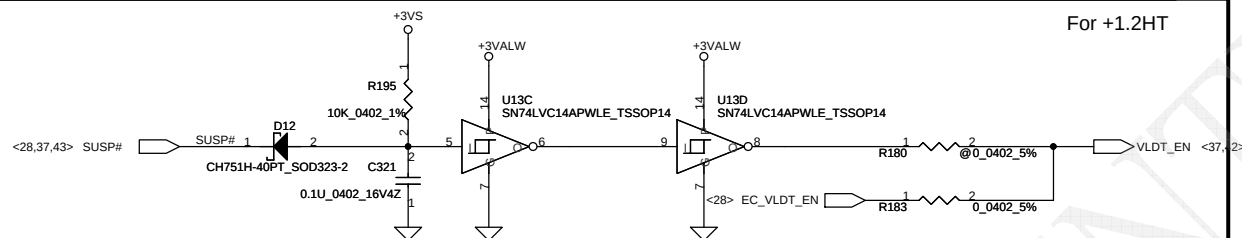
For South Bridge



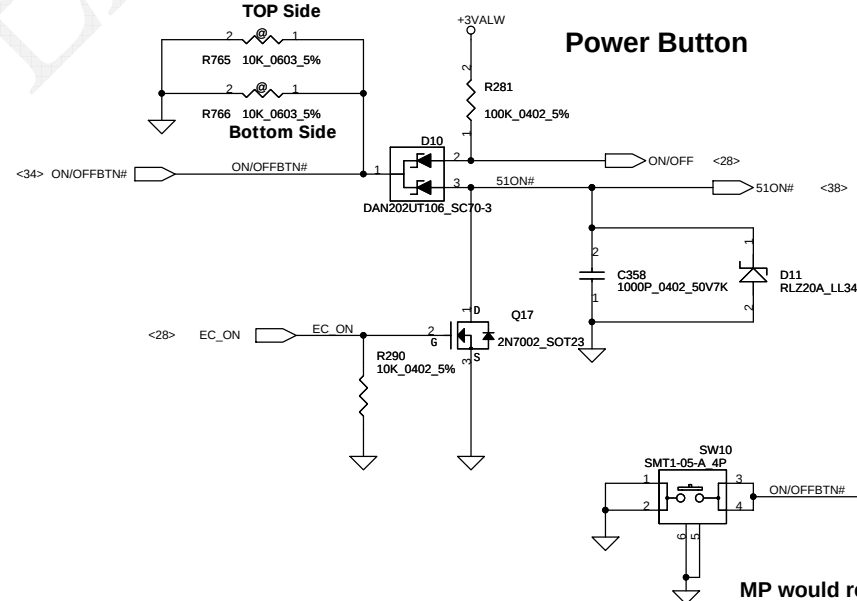
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



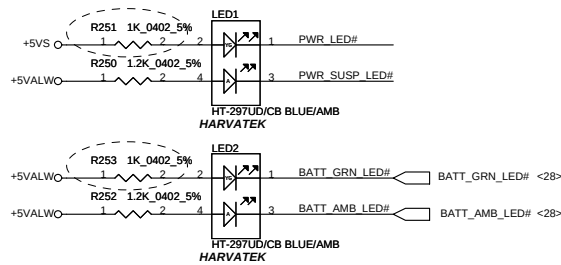
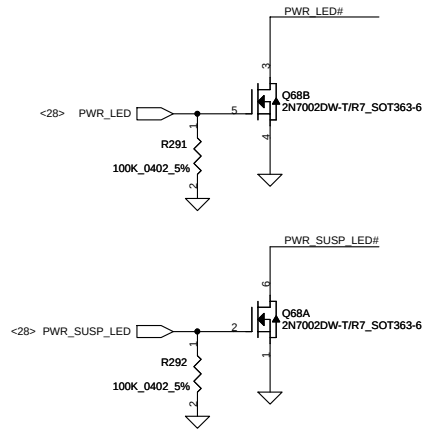
For +1.2HT



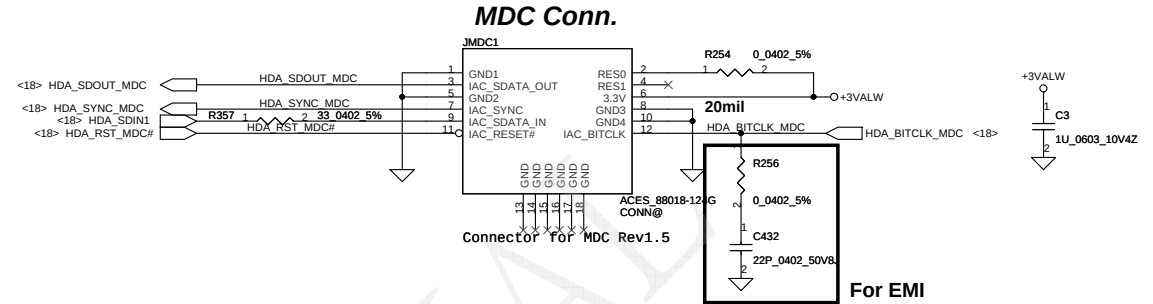
TOP Side



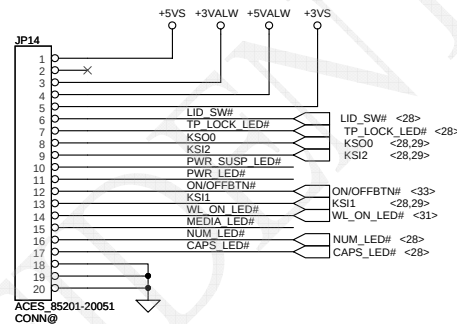
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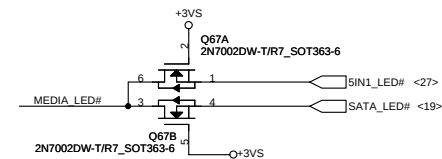
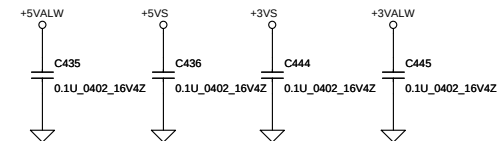
BLUE/AMB LED



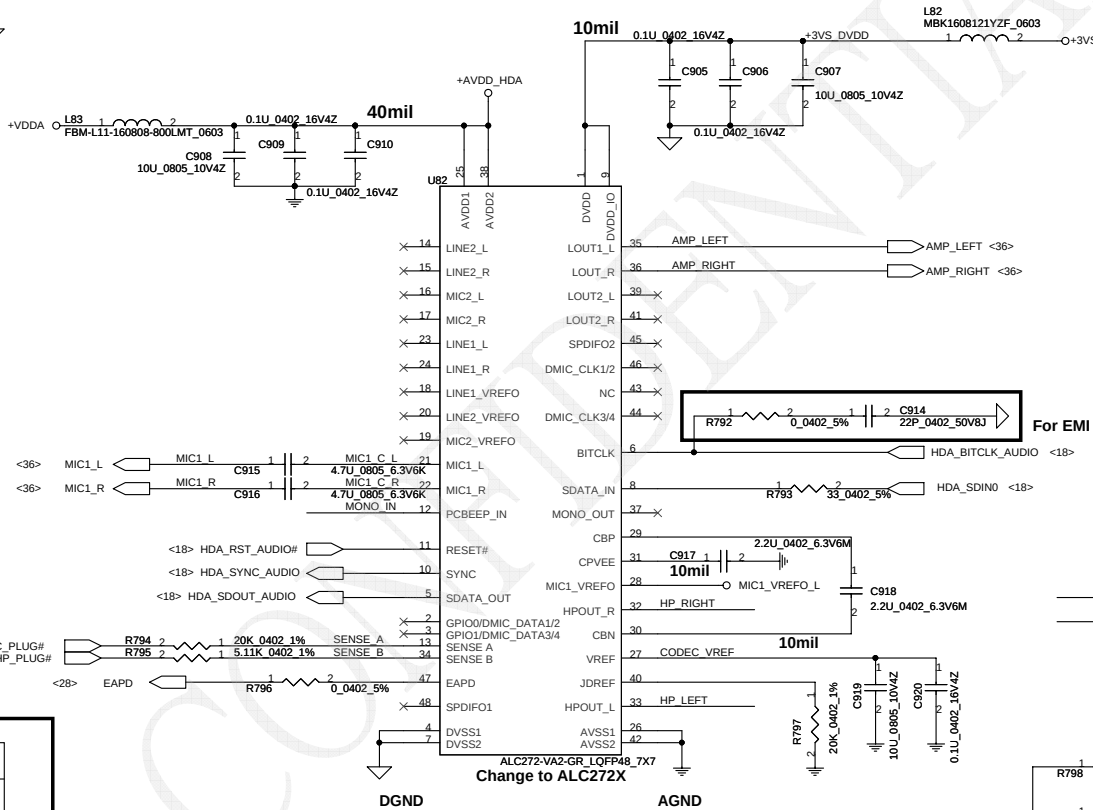
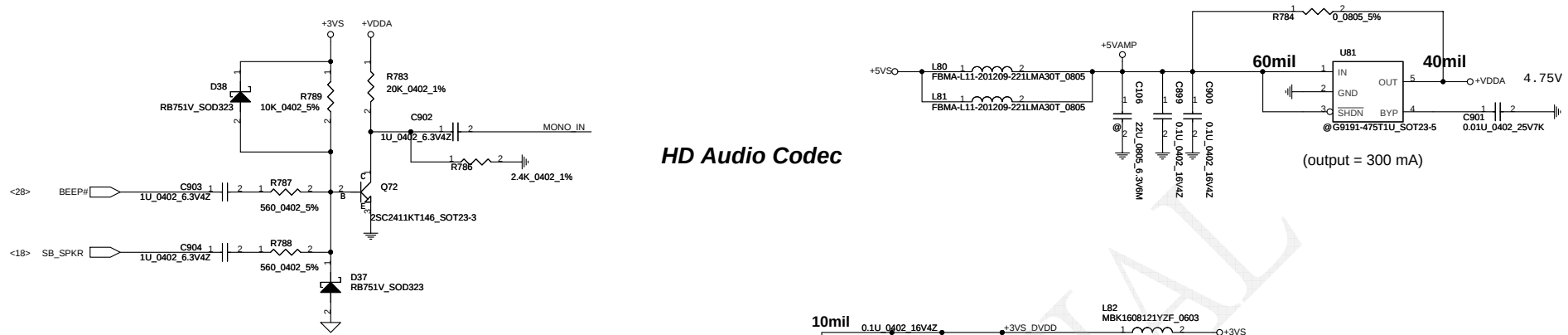
To PWR LED/B



	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



HD Audio Codec

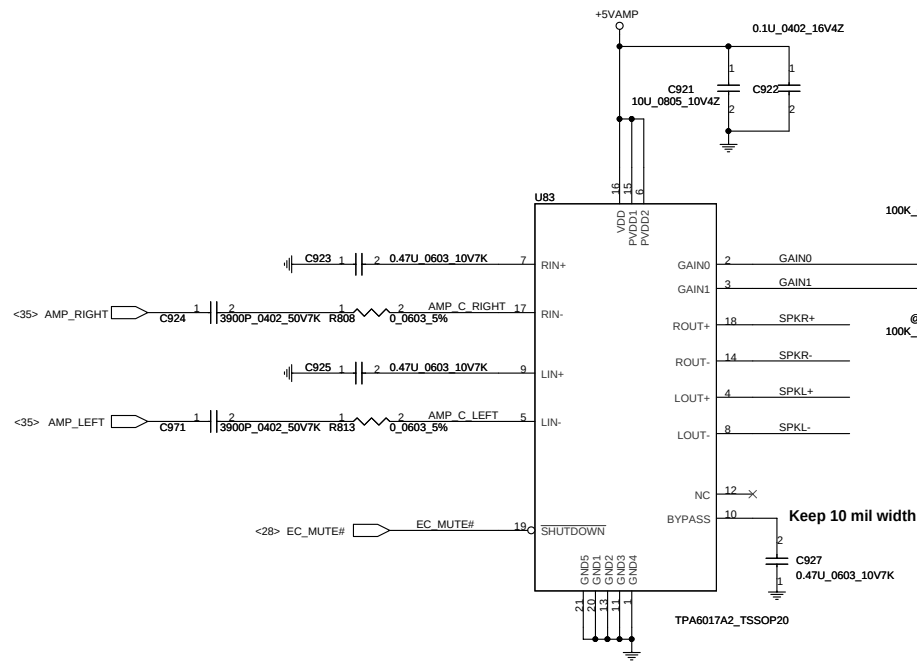


update this table

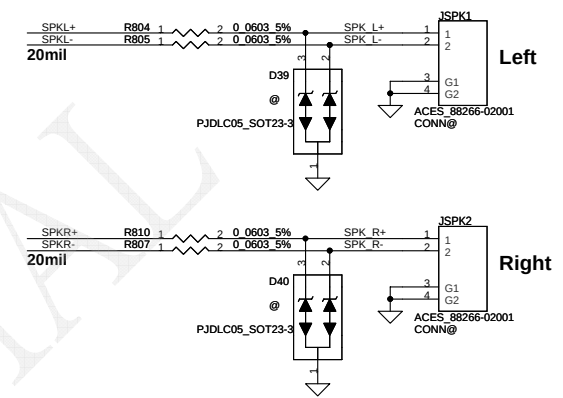
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Change to ALC272X

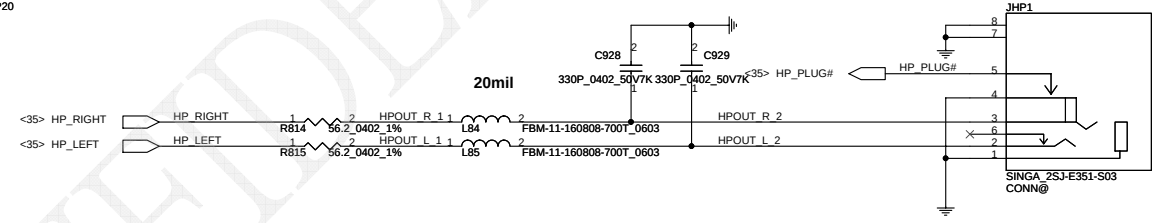
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2010/03/12				Title				SCHEMATIC, MB A5991			
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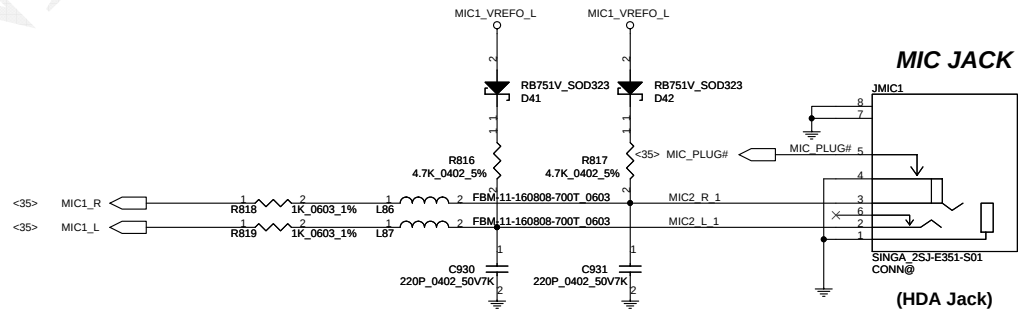
Int. Speaker Conn.



LINE Out/Headphone Out



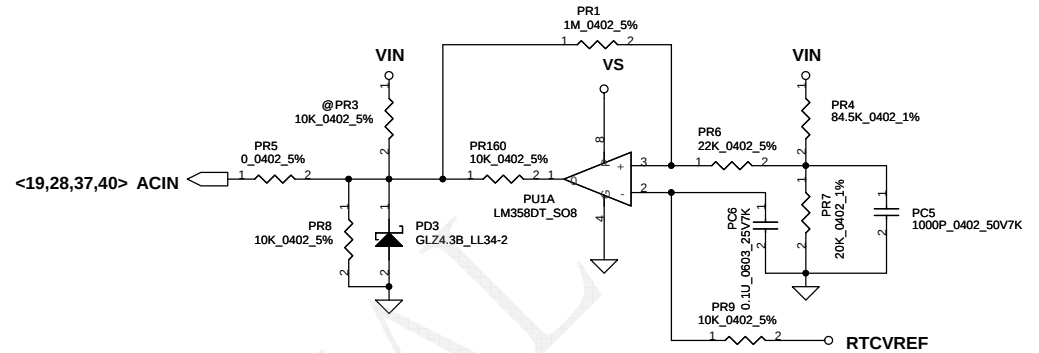
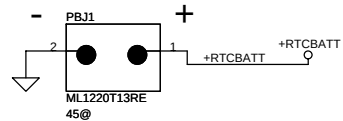
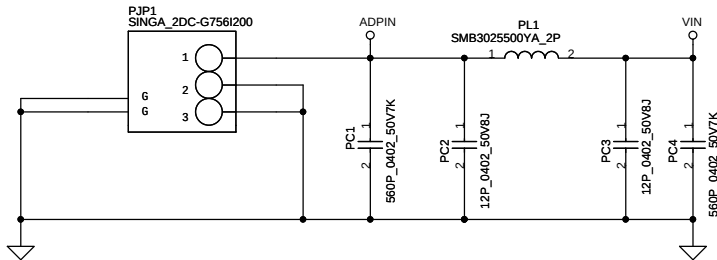
MIC JACK



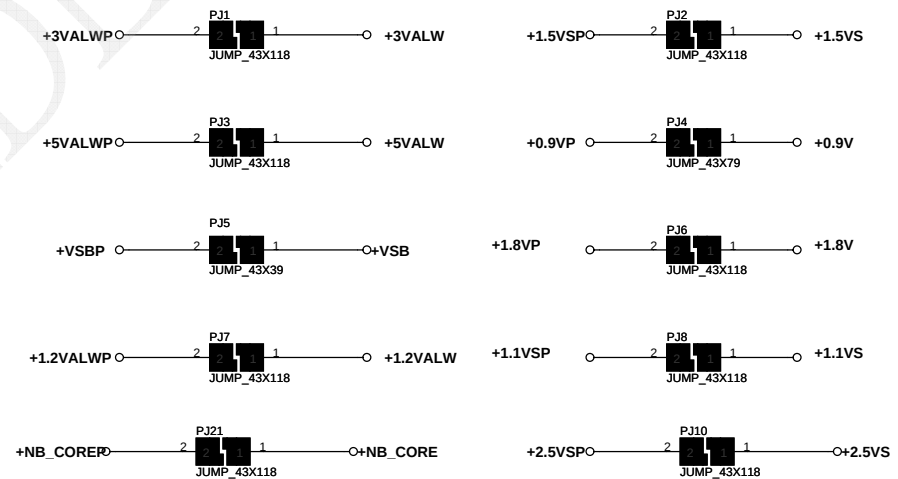
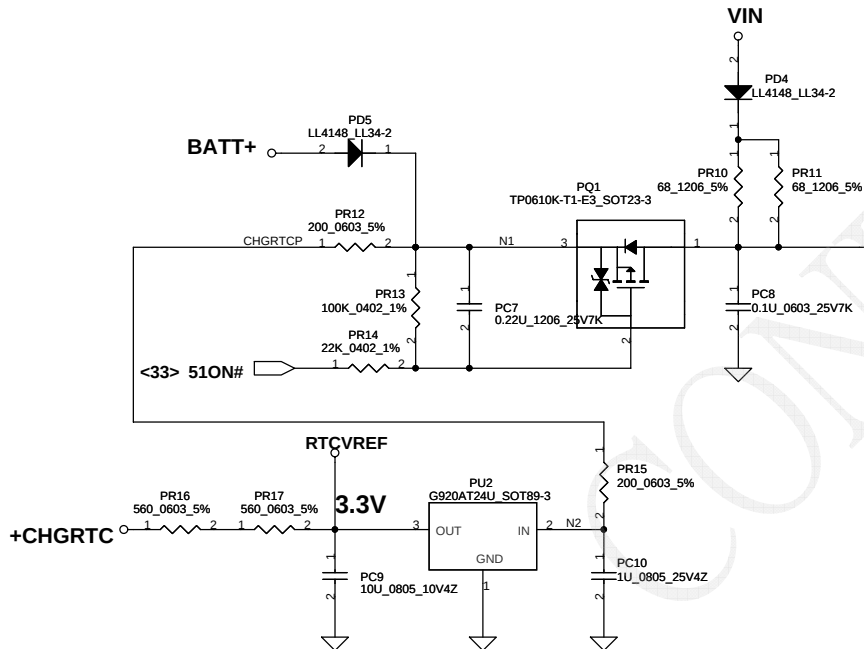
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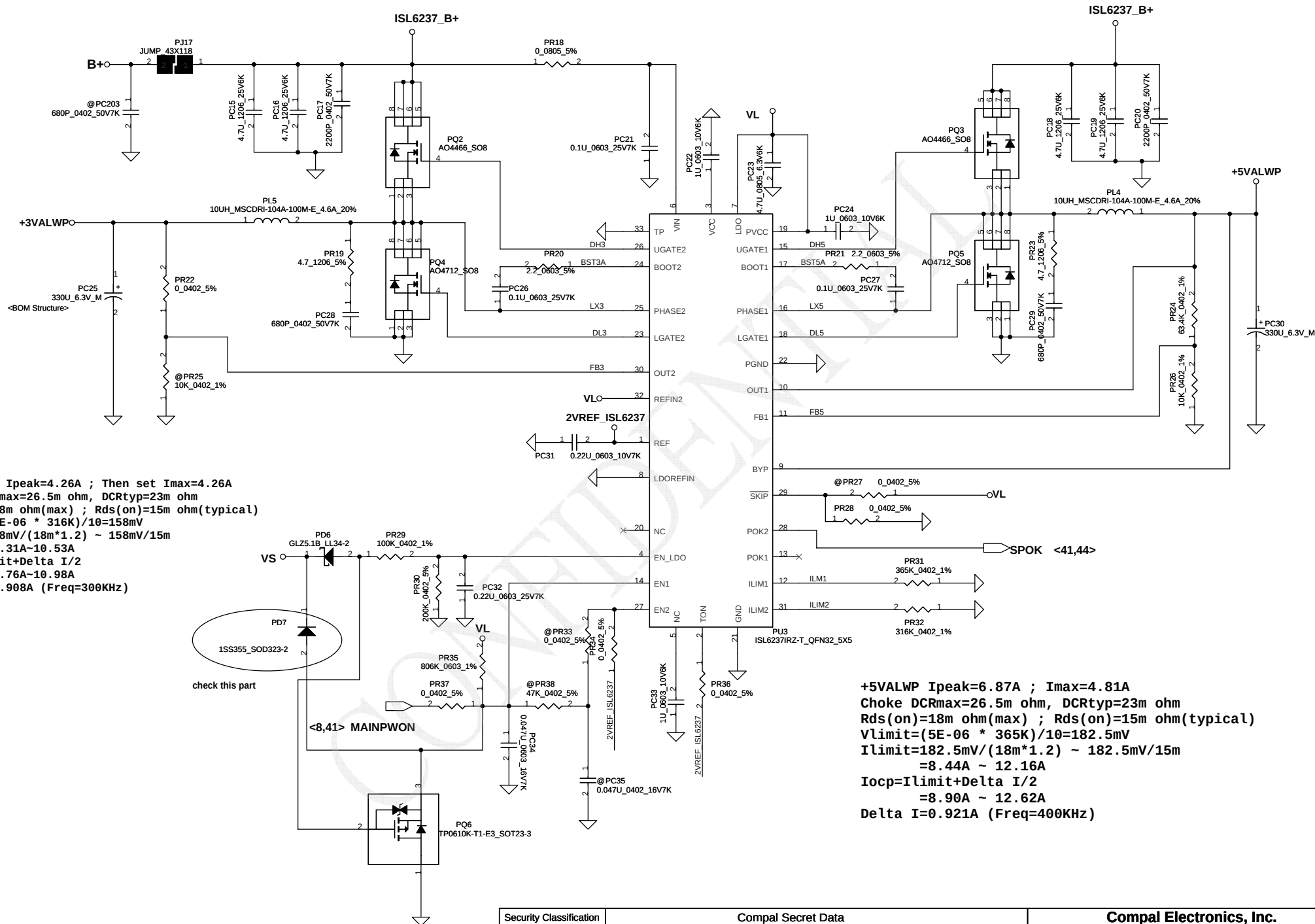
DC231000500



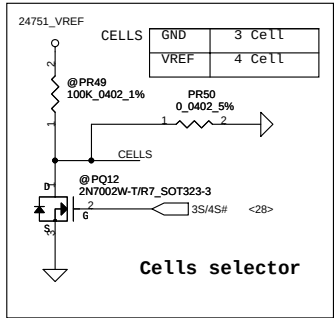
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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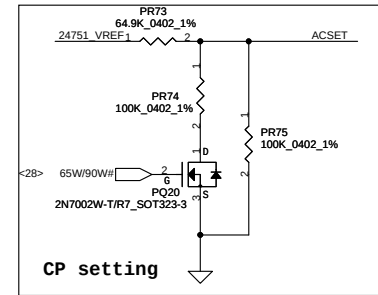
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Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

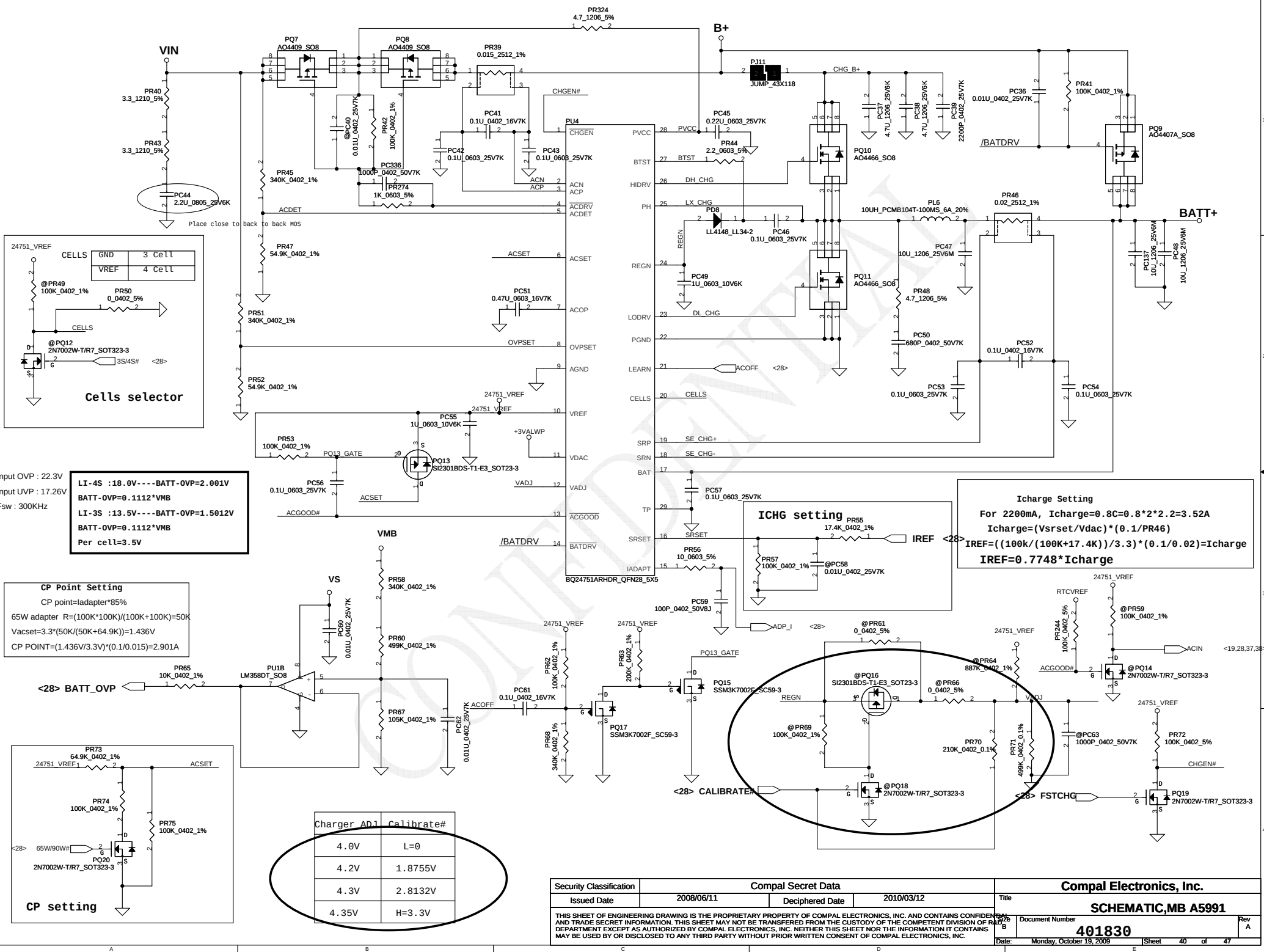
LI-4S : 18.0V --- BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S : 13.5V --- BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

CP Point Setting
 CP point=ladapter*85%
 65W adapter R=(100K*100K)/(100K+100K)=50K
 Vacset=3.3*(50K/(50K+64.9K))=1.436V
 CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A

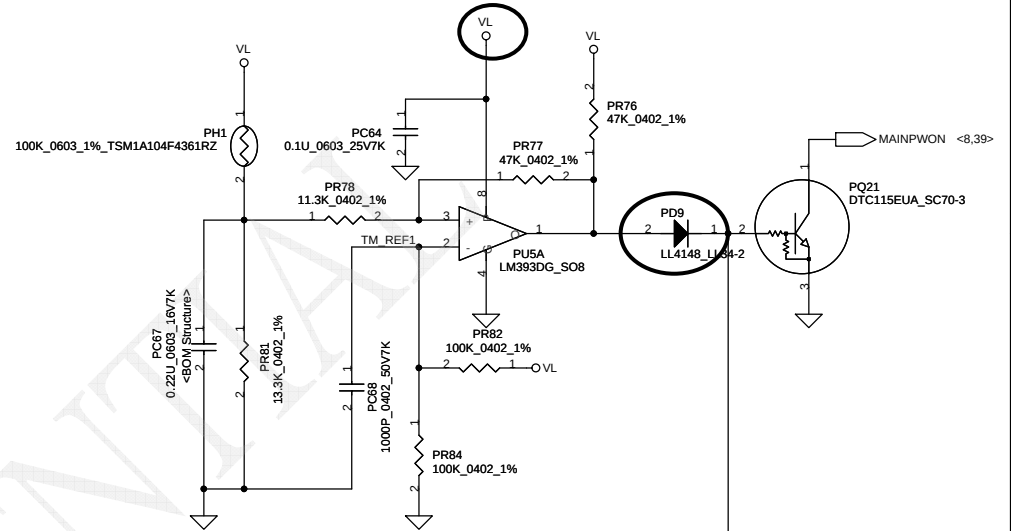


Charger AD1 Calibrate#

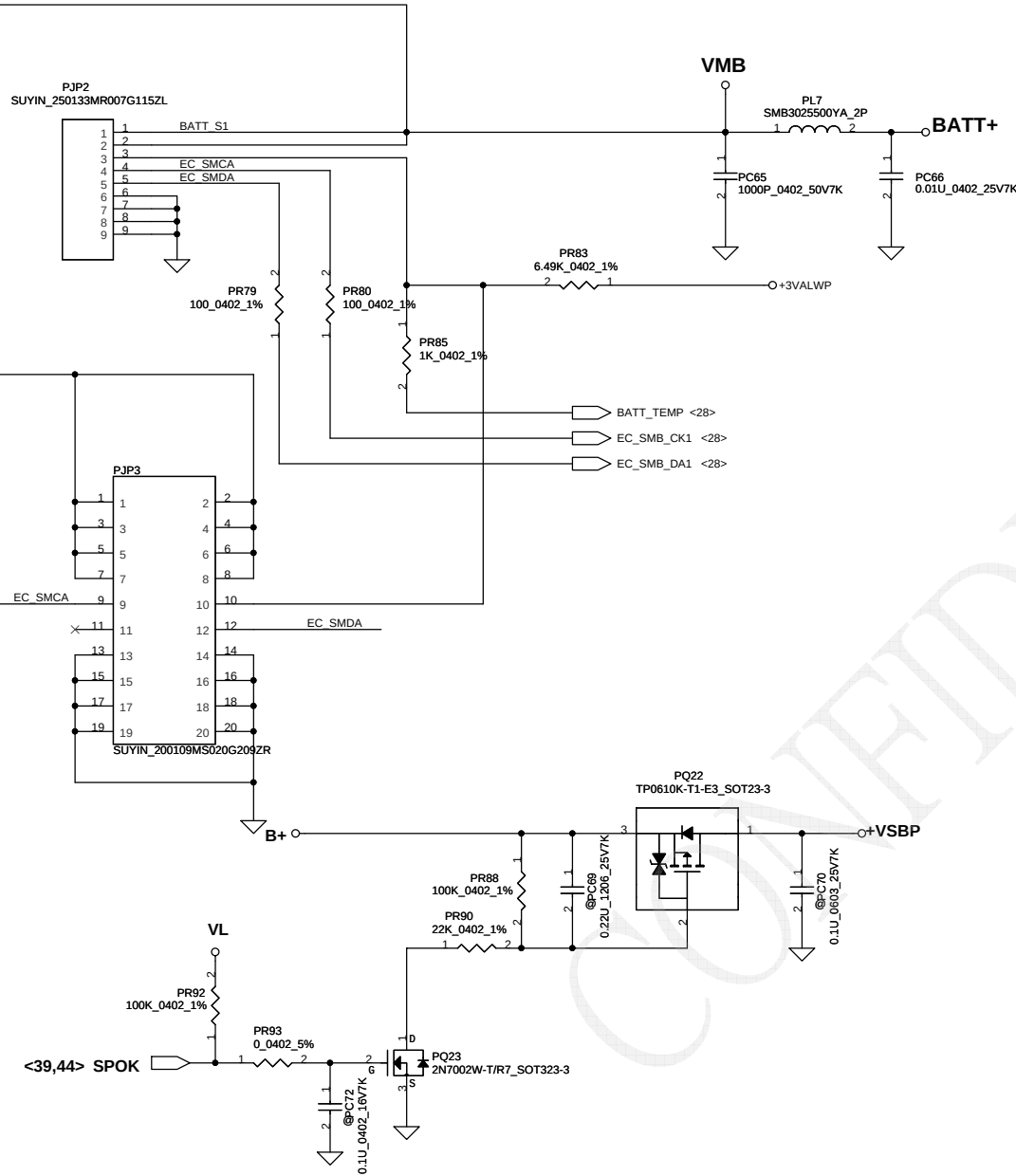
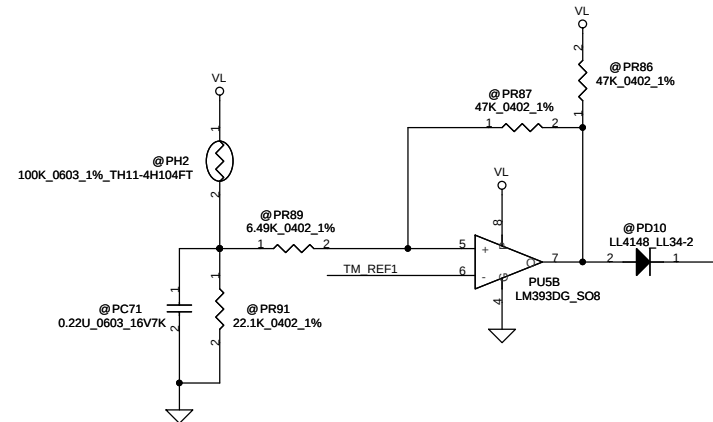
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V



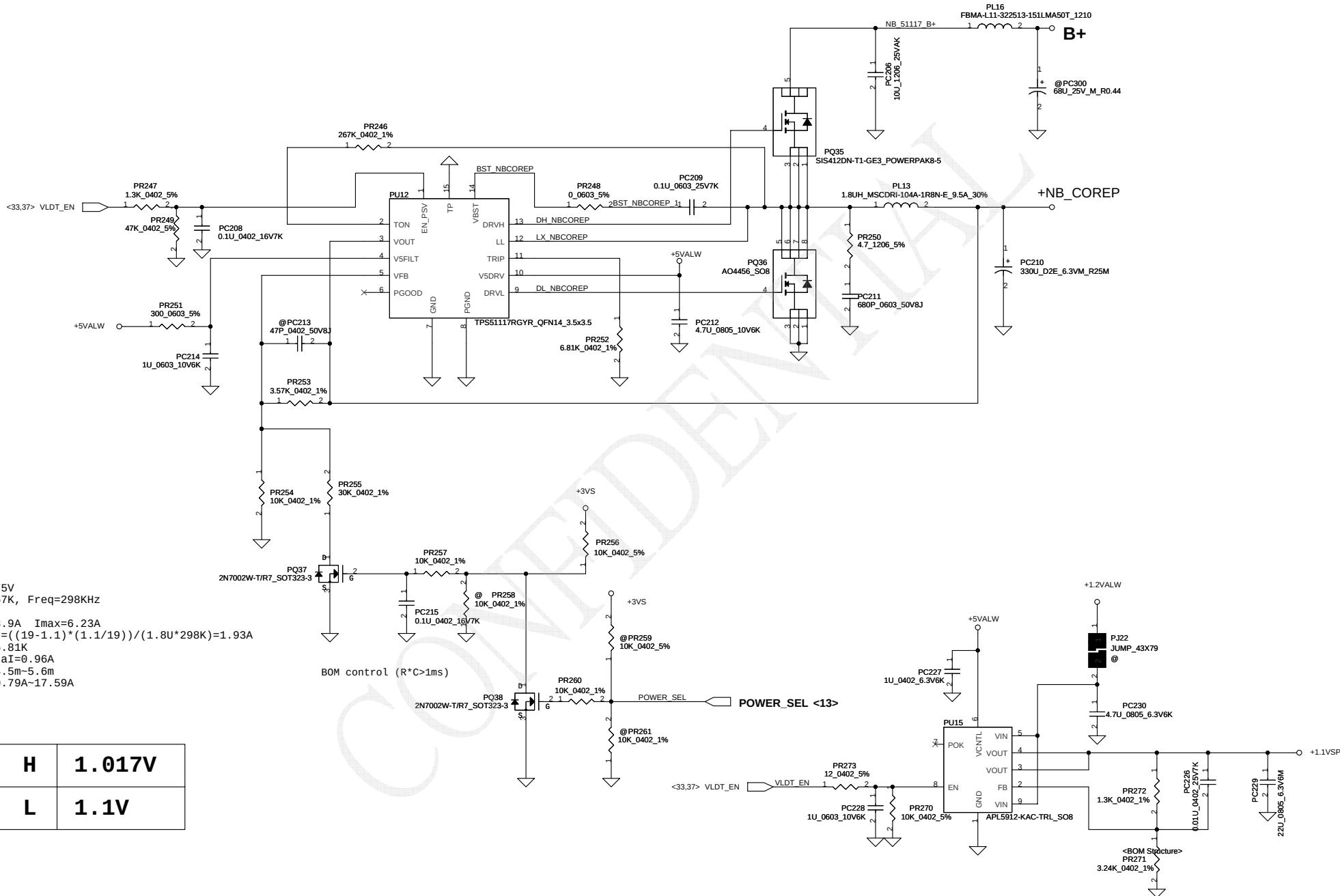
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C

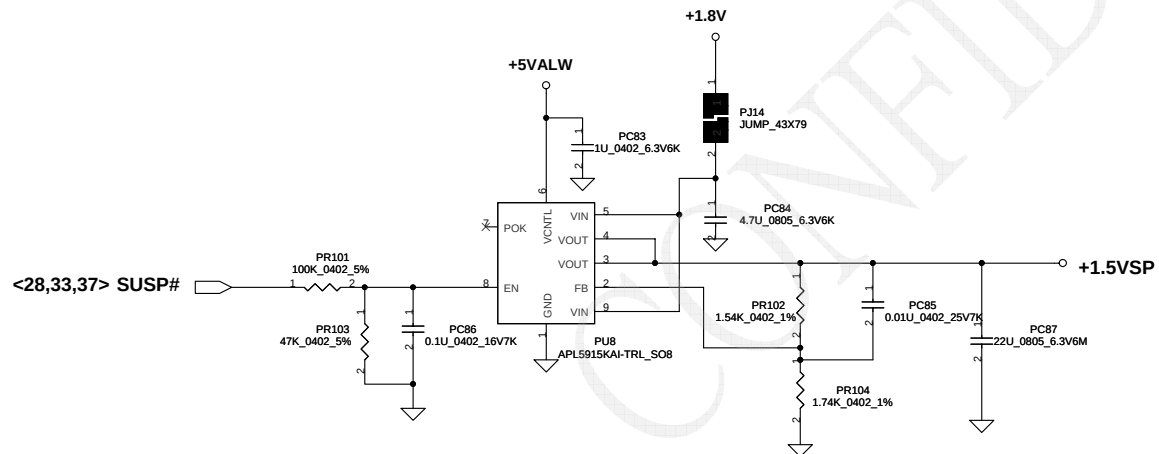
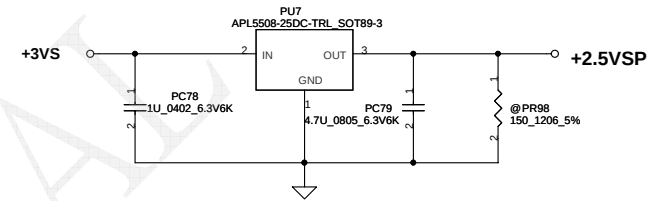
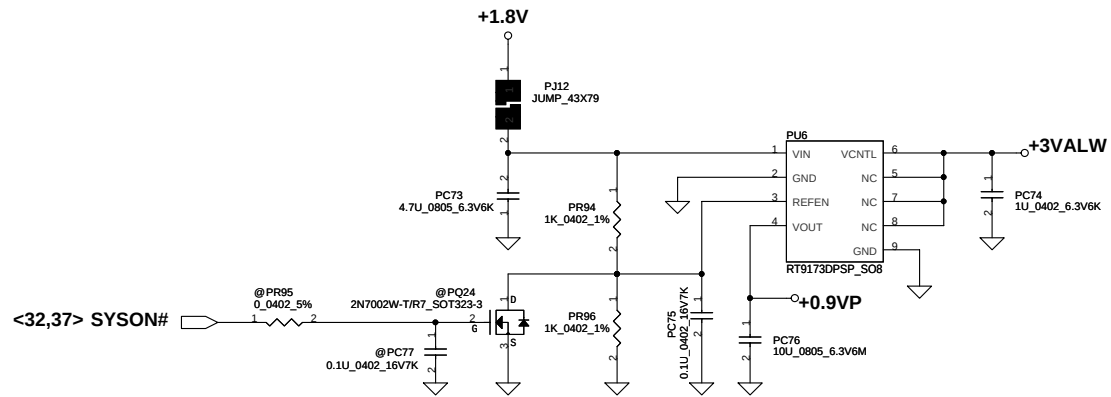


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H	1.017V
L	1.1V

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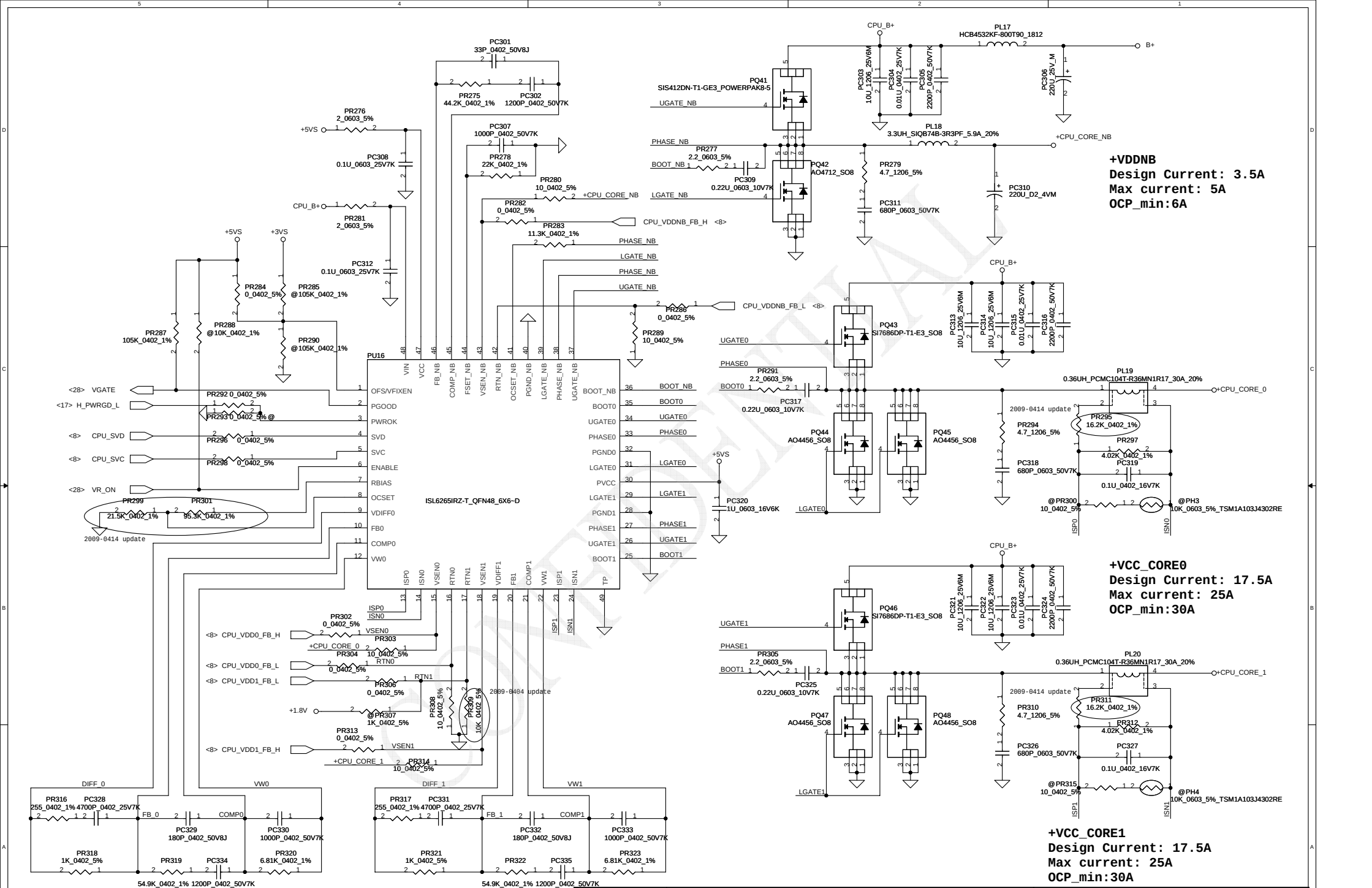
VFB=0.75V
Vo=VFB*(1+PR111/PR112)=0.75*(1+14K/10K)=1.8V
Rton=267K=>Faw=297KHz

Cout ESR=15m ohm
Ipeak=11.96A, Imax=8.372A
Delta I=((19-1.8)*(1.8/19))/(L*Fsw)
((19-1.8)*(1.8/19))/(1.8u*297000)=3.048A
=>1/2DeltaI=1.524A
Rtrip=9.76K
Iocp=15.20A-24.71A

VFB=0.75V
Vo=VFB*(1+PR119/PR120)=0.75*(1+6.04K/10K)=1.203V
Rton=267K=>Fsw=298KHz

1.2VP Ipeak=7.4A ; Imax=5.180A
Delta I=((19-1.2)*(1.2/19))/(L*Fsw)
((19-1.2)*(1.2/19))/(1.8u*298000)=2.10A
=>1/2DeltaI=1.05A
Rdson=15m/18m ohm
set Rtrip=8.66K
Icop_min=4.77A
Icop_max=7.74A

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